ECS Transactions, 33 (3) 367-374 (2010)
10.1149/1.3481625 ©The Electrochemical Society

Maxwell-Wagner Instabilities and Defects Generation during CVS in REO-HfO_2 Gate Stacks Grown on Germanium Based MOS Devices

M. S. Rahman[a,b,1], E. K. Evangelou[b], and A. Dimoulas[c]

[a] GSI - Helmholtzzentrum für Schwerionenforschung, Darmstadt 64291, Germany
[b] Lab. of Electronics-Telecoms. & Applications, Department of Physics, University of Ioannina, Ioannina 45110, Greece
[c] MBE Laboratory, Institute of Material Science, DEMOKRITOS, Athens 15310, Greece

The Current Instabilities and defect generation during constant voltage stress (CVS) in REO-HfO_2 gate stacks grown on Ge (001) substrates by molecular beam deposition are extensively studied, and analyzed. Due to the different conductivities of the dielectrics in gate stacks, charge accumulates at the interface of the stack thus resulting in current decay, which can be explained by the simultaneous effects of the Maxwell-Wagner instability and dielectric relaxation. Moreover, under CVS conditions new defects are created which is evident from 'Border traps' analysis.

Introduction

Gate stacks using Rare-earth oxides (REOs, e.g. CeO_2, Dy_2O_3, La_2O_3) as an interfacial buffer layer can be effectively grown on Ge substrates demonstrating better passivation and electrical properties (1). However, it is imperative to study a number of reliability concerns such as, accumulation of charge at the interface of the two dielectrics, charge trapping, defect generation and stress-induced leakage current (SILC) within each layer as well as oxide degradation issues to understand completely the quality of the corresponding gate stacks (2, 3, 4).

Usually, gate stacks configurations for future MOS technology consist of two layers namely, a buffer layer with better structural and interfacial properties and a high-κ layer (Hf or Zr oxide) which gives the desired insulating and dielectric properties. These two different layers will also have different conductivities, so charge will accumulate at the corresponding interface until, in steady state, the same current density flows through both layers. The effect is called Maxwell-Wagner polarization (M-W) and causes significant current instabilities (2). Another detrimental phenomenon in modern MOS devices is charge trapping, which is observed in most high-κ dielectrics either in a single or gate stack configuration (5, 6, 7). Both effects lead to oxide degradation in ultrathin dielectric layer subjected to high-field stress which is critical in ULSI technology. As a matter of fact, charge trapping in the dielectrics often is used as a monitor of degradation (6), it causes threshold voltage ΔV_{th} shifts and drive current degradation over device operation time (6, 7).

Furthermore, dielectric relaxation in a solid is a bulk-related phenomenon, which causes relaxation current following the direction of dV/dt. (8, 9). When an external field

[1] *corresponding author's email: M.S.Rahman@gsi.de (M. Shahinur Rahman)*

is applied across a film, it separates the bound charges and results in polarization and a compensating internal field. Also when the external field is released, the internal bound charges are neutralized by the hopping of free charges, while a remnant polarization and an internal field are still present in the film (8). However, Cester, et. al. (10) explained the decay of stress-induced current with time by two mechanisms, namely, either a local relaxation of the lattice, or a weak spot "clogging" of the oxide neutral defects by injected electrons. The accumulation of charge at the interface of a bilayer gate stack stimulates dielectric relaxation effects in each layer. In general, relaxation is a slow process and the relaxation current decays with time following the Curie–von Schweidler (C-S) law [9]: $J = P.C/t^n$, where J is the relaxation current density (A/cm^{-2}), P is the total polarization or surface charge density (V nF/cm^{-2}), t is time (s), C is a constant, and n is a real number close to unity. It is rather perplexed to appraise the stress-induced defects generation in high-κ dielectrics as a high density of as-grown defects in transition metals (11, 12) and in a gate stack keeping a REOs layer at the interface between the high-κ dielectrics and the Ge substrates (1, 2, 3).

In this paper we report on the various reliability issues such as Maxwell-Wagner (M-W) current instabilities and defects generation in REOs-HfO_2 gate stack structures during CVS at accumulation.

Experimental

The CeO_2, Dy_2O_3, La_2O_3 and HfO_2 films used in the present study, were prepared by Molecular Beam Deposition (MBD) on both *n*-/*p*-type Ge (001) substrates with a resistivity of 1.6–1.9 Ω-cm. Prior to deposition, all samples were annealed at 360-400 °C for several minutes until a clear (2x1) reconstruction pattern appeared, indicating a clean Ge surface. The oxides were subsequently deposited at 360^{o}C (La_2O_3), 225^{o}C (Dy_2O_3), 225^{o}C (CeO_2). As-deposited samples were used for this study. Thicknesses of the samples were estimated by X-ray reflectivity measurement. The top gate electrode was prepared by e-beam evaporation of 30-nm-thick Pt using a shadow mask to define circular dots 300 μm in diameter (corresponding area A=7x10−4 cm^2), while the back ohmic contact was realized using an eutectic In–Ga alloy. The capacitance voltage (C–V_g), current versus time (J_g–t), and current versus gate voltage (J_g-V_g) characteristics of the MOS capacitors were studied using an Agilent 4284A LCR meter, a Keithley 617 electrometer, and appropriate programming. More details can be found elsewhere especially for the 'stress and sense technique' (3, 4, 7). All the measurements were done in a dark box and at room temperature. Fresh devices were used for each stress measurement. The maximum variation of temperature during the experiment never exceeded ±0.5 ^{o}C.

Results and Discussion

The gate stacks of REOs-HfO_2 grown on Ge substrates under MBD technique in the present study show improved electrical characteristics which have been reported elsewhere (13, 14). In the present work though, we report merely on the reliability issues of the corresponding gate stacks. For investigating the current transient characteristics of Dy_2O_3/HfO_2/*p*-Ge MOS devices we apply different CVS bias (from -1 to -4V) always in accumulation. The corresponding current densities as a function of stress time (J_g-t) curves are shown in Fig.1. At low CVS conditions, Fig. 1 illustrates a current decay with respect to stress time following a power law (t^{-n}). On the contrary, at higher CVS we do

not notice dielectric relaxation, because the charge trapping mechanism dominates as will be discussed in a later section. Soft breakdown (SBD) and hard breakdown (HBD) events have also been detected at higher bias fields and/or prolonged stress time as in the plot. For the case of the single layer REO devices, similar behavior have been reported earlier, that is, current decay was observed at low CVS conditions whereas at high stress field charge trapping was observed together with the creation of new defects within the bulk of the dielectric layers (3, 15). It is worth mentioning here that REOs form germanate interfacial layers in contact with Ge so, it is reasonable to assume that they also behave as a bilayer dielectric stack.

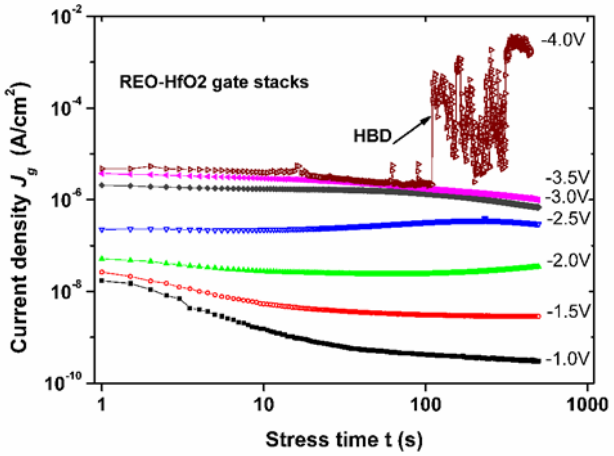

Fig. 1. Evolution of Current with time (J_g-t transient) at various CVS conditions in Dy_2O_3 (2nm)-HfO_2 (5nm) gate stacks, grown on Ge substrates. At low CVS current decay is observed which is indicative of dielectric relaxation ($J \sim t^{-n}$) behavior; moreover the progressive breakdown (PBD) is noticed at high CVS which eventually leads hard breakdown (HBD) of the device.

Fig.2 illustrates the current density J_g versus stress time t curves of a Dy_2O_3/HfO_2 gate stack during CVS at accumulation (Vg = -3V), while after each J_g-t stress the J_g-V_g curve was also monitored. It is evident that in all cases the decay of current follows a power law ($J \sim t^{-n}$) with an n value ranging from 0.7 to 0.9. The n values increase after each new stress cycle, reaching a value of 0.9 after ten successive cycles of 500s each. The The fact that the initial value of n (=0.7) is far from unity for the first stress cycle indicates that a Maxwell–Wagner (M-W) instability (following the terminology after Ref. 2) is present along with C-S dielectric relaxation of the high-k dielectrics. However, after ten consecutive stress cycles (500s each) the current decays with time following C-S law. The gradual increase of n could be attributed to the fact that the Maxwell–Wagner instability becomes less important after each stress cycle and the relevant J_g values decrease so that, after ten consecutive cycles, it is the dielectric relaxation current that dominates as illustrated in Fig. 3. One reason for that is the gradual change of the conductivities of the various dielectric layers due to charge trapping in pre-existing bulk oxide defects. In order to study this behaviour a set of measurements have been performed on fresh devices with Dy_2O_3/HfO_2 gate stacks. The experimental data (fig. 3) followed nicely a model proposed by Jameson *et al.* (2) which considers both Maxwell-Wagner instability (M-W) and dielectric relaxation. It is interesting to point out that neither mechanism alone (C-S or M-W) could fit the experimental data.

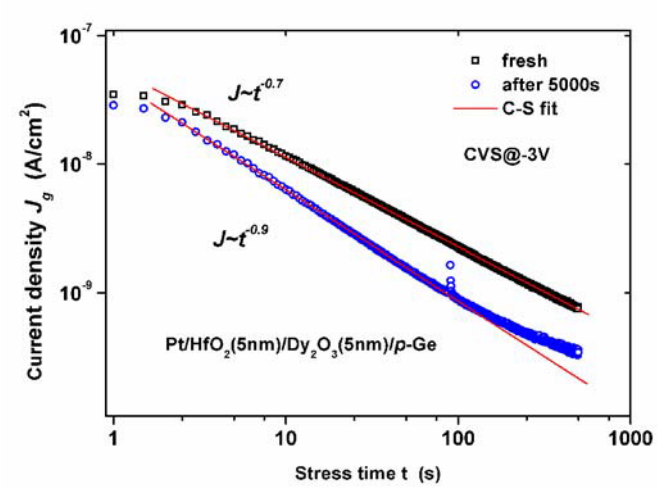

Fig. 2. J_g-t transients (current density vs. stress time) characteristics of Dy_2O_3(nnm)/HfO_2(nm) stacks grown on p-Ge substrates during CVS at V_g=-3V. Each stress cycle was 500s, while black (square) and blue (circle) dots represent the first and last out of ten successive cycles, and the solid line represents the Curie-von Schweidler (C-S) relaxation fit to experimental data.

In Fig. 3 the dotted line (blue) is the theoretical curve (not fitted to experimental data) of C-S relaxation, it is obvious that the experimental data is well described when M-W instability is considered, and the fit (red solid line) proves the M-W current instabilities is exist in the dielectric gate stacks.

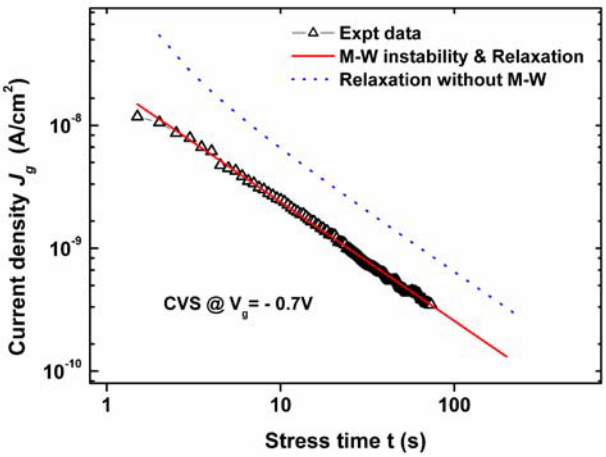

Fig. 3. The solid line (red) is best fit to experimental data (J_g-t curve) of Dy_2O_3 (2nm)/HfO_2(5nm) gate stacks. A model based on the simultaneous effects of M-W and C-S relaxation instabilities (see *Ref.2*) fits the data nicely; however only relaxation model (dotted line) can not fit data.

Another interesting concept that of "border traps" was originally introduced by Fleetwood, et al (16) as a new subclass of defects commonly appearing in MOS devices. These defects lie physically within the oxide but are near enough to the semiconductor/oxide interface, and they often act indistinguishably from interface traps which are also termed "near-interface traps". The effective border trap density can be obtained from C–V_g hysteresis (17, 18) and is given by the following equation:

$$\Delta N_{bt} \approx \frac{1}{qA}\int\left|C_r - C_f\right|dV \qquad [1]$$

The C–V_g difference curve $C_{rf}(V) = (C_r - C_f)$ is a function of the applied gate voltage. The indexes refer to measurement from accumulation to inversion ($C_r = C_{\text{reverse}}$) and inversion to accumulation ($C_f = C_{\text{forward}}$). The border traps analysis C_{rf} *(V)* curves of single REOs and REOs-HfO2 gate stacks are shown in Fig. 4 (a) and (b) respectively. The C-V_g curves were taken at f=100kHz, with a ramp rate of ~0.1 V/s, corresponding to switching times of ~ 40 s over the portion of the curve showing hysteresis. Usually, they are strongly peaked functions, going to zero above flatband or below inversion (16, 18).

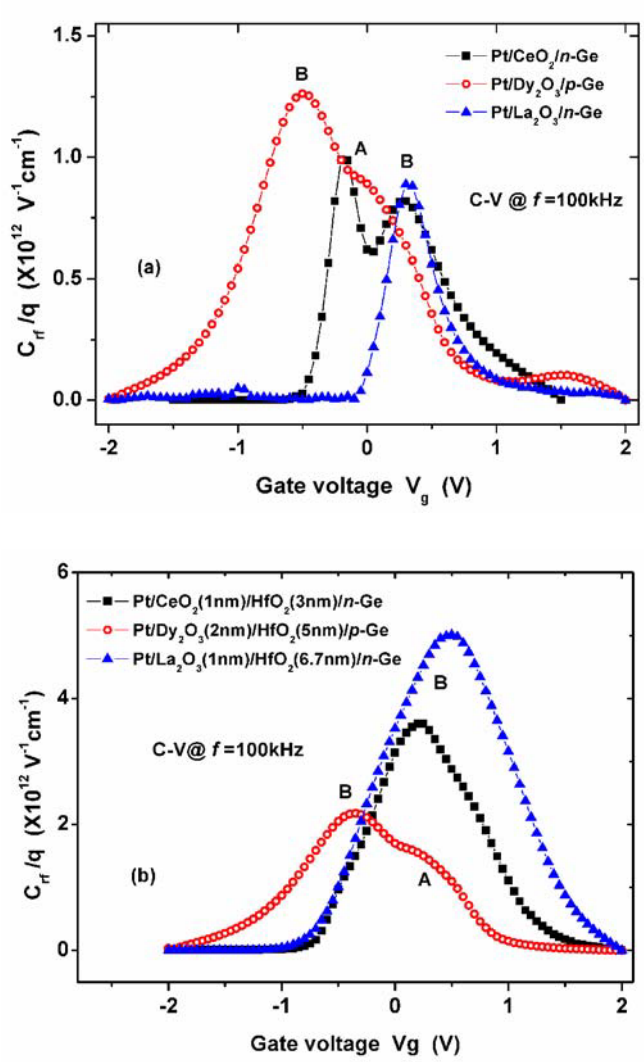

Fig. 4. C_{rf} (the difference in capacitance between the forward and reverse curves of high frequency C-V @ 100 kHz) vs. gate voltage curves of (a) rare-earth oxides (REO, i.e. CeO_2, Dy_2O_3, La_2O_3), and (b) REO-HfO_2 gate stacks. The area under each curve is proportional to the total number of "border traps" ΔN_{bt}. The points A and B represent interface traps and 'Border traps' respectively.

In the data shown in Fig. 4(a), one peak (A) lies in the depletion region for CeO_2 and Dy_2O_3 whereas for La_2O_3 no peak lies in the depletion, where mainly the interface traps respond. Another peak (peak B) lies for all REO based stacks, in strong accumulation (15). The deformation (peak) of the $C_{rf}(V)$ curves in accumulation is commonly attributed to excess charge ('border traps') trapped throughout the oxides (e.g. CeO_2, Dy_2O_3), and is absent for the case of La_2O_3 which indicates better dielectric behaviour in terms of (less) charge trapping. In Fig. 4(b) both La_2O_3 and CeO_2 gate stacks are strongly peaked at accumulation illustrate no excess charge trapping, and this could well be due to the 1nm interfacial layer that completely form La/Ce-Ge-O i.e. germanate interfacial layers (13, 19) is sign of good integrity in gate stacks composition. Whereas for the case Dy_2O_3/HfO_2 gate stack the Dy_2O_3 layer is rather thick (2nm) forms GeO_2 interfacial layer (<1nm) with Ge substrates (14), and that could be the reasons having two peaked curve that is excess amount of charge trapping. One thing to emphasise here that the current density (V_{FB}±-1V) of Dy_2O_3/HfO_2 gate stack (14) is lower than that of CeO_2/HfO_2, La_2O_3/HfO_2 gate stacks (13) which is consistent with the interfacial characteristics of these gate stacks.

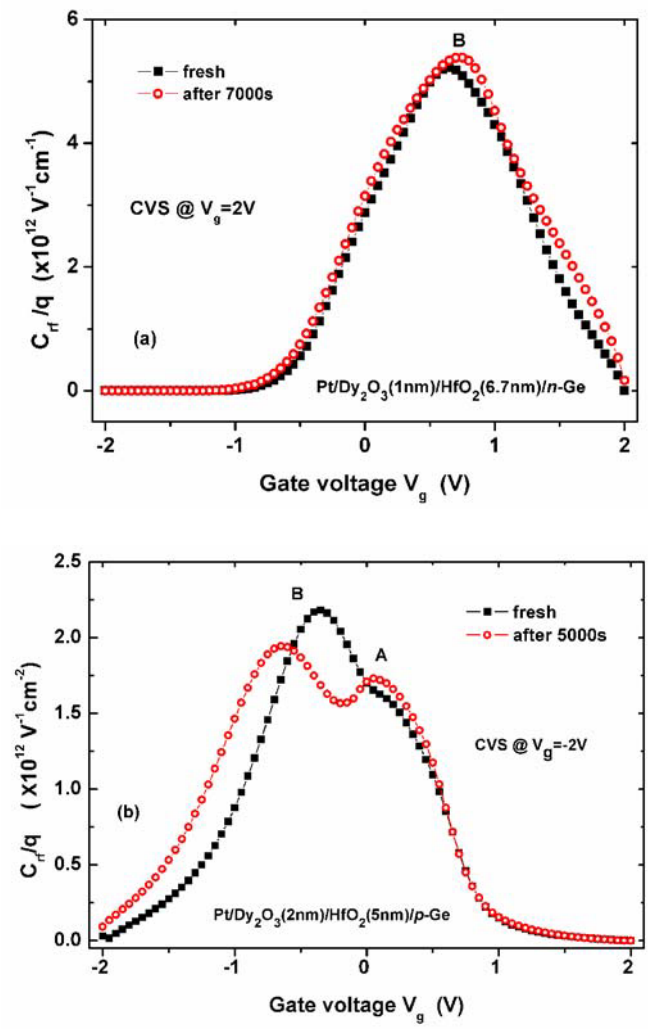

Fig. 5. Plots illustrate the evolution of 'border traps' in (a) La_2O_3/HfO_2, (b) Dy_2O_3/HfO_2 gate stacks under constant voltage stress (CVS) conditions. Total number of 'Border traps' increases with the progress of time (stress time) during CVS in both gate stacks.

Figs. 5(a, b) show the evolution of newly created border traps during the application of a CVS pulse at accumulation in La_2O_3/HfO_2 and Dy_2O_3/HfO_2 gate stacks. In both cases the C_{rf} curve shapes are not the same and this could be due to different integrity of the gate stacks and/or type traps created in the dielectrics. The important experimental result from this study is the creation of new border traps with a density proportional to the stress time under CVS.

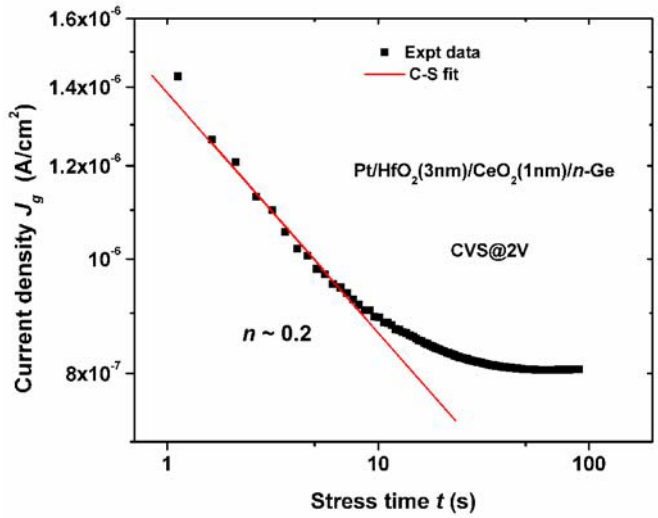

Fig. 6. Current density J_g vs. stress time t of CeO_2/HfO_2 shows the current decay characteristics.

A typical time–decaying J_g-t curve of $CeO_2/HfO_2/n$-Ge during CVS bias is shown in Fig. 6. By fitting a power law (C-S) an n~0.2 value was extracted, which signifies the creation of new defect when the device is under bias. This behavior of current decay could also be explained by a common 'field lowering' model (4). For the case of La_2O_3/HfO_2 gate stacks, during the application of low stress bias, charges accumulated at the interface of the bilayer as well as charge trapped on preexisting traps in the bulk, lower the internal field and cause current decay. In that study (*Ref.4*) the n value extracted as n~0.7 at low pulse (CVS@ 0.5V) while n~0.15 at higher field (CVS@ 2.4V), from which it is evident that due to high field bias new defects are created and n value decreases.

Conclusions

Current instabilities such as Maxwell-Wagner (M-W) and dielectric relaxation (C-S) as well as defect generation were extensively studied on Ge based MOS devices with gate stack dielectrics. It is evident that M-W and C-S relaxation instabilities are acting simultaneously on the REOs-HfO_2 bilayer dielectrics when the devices are under bias. Although the gate stacks grown on Ge substrates show better electrical characteristics, in terms of reliability issues high-κ bilayer gate stacks itself is the cause of charge trapping/accumulation at interfaces of two high-κ layers and the creation of new defects are the crucial concern to be understood deeply before using in as MOS devices.

Acknowledgments

One of the authors, M.S.R would like to thank the Marie-Curie Postdoctoral Fellowship (MC-PAD) and the Greek state scholarship (IKY) for the financial supports.

References

1. A. Dimoulas, M. Houssa, A. Ritenour, J. Fompeyrine, W Tsai, J.W. Seo, ECS Trans., **3**, 371 (2006).
2. J. R. Jameson, P. B. Griffin, J. D. Plummer, and Y. Nishi, *IEEE Trans. Electron Devices*, **53,** 1858(2006).
3. M. S. Rahman, E. K. Evangelou, I. I. Androulidakis, A. Dimoulas,G. Mavrou, and P. Tsipas, *J.Vac. Sci. Technol. B*, **27**, 439 (2009).
4. E. K. Evangelou, M. S. Rahman, A. Dimoulas, and S Galata, ECS Trans, **25**(6), 105(2009).
5. P. P. Apte, and K.C. Saraswat, *IEEE IPRS 1994*, 136 (1994).
6. E. P. Gusev, and C. P. D'Emic, *Appl. Phys. Lett.*, **83**(25),5223(2003).
7. M. S. Rahman, E. K. Evangelou, A. Dimoulas, G. Mavrou, and S. Galata, *J. Appl. Phys.*, **103**, 064514(2008).
8. W. Luo, Y. Kuo, and W. Kuo, *IEEE Trans. Device Mater. Rel.*, **4**(3), 488(2004).
9. A. K. Jonscher, *J. Phys. D, Appl. Phys.*, **32**(14), R57(1999).
10. A. Cester, A. Paccagnella, and G Ghidini, *Solid-State Electron.*, **45**, 1345(2001).
11. G. Bersuker, P. Zeitzoff, G. A. Brown, and H. R. Huff, *Mater. Today,* **7**, 26(2004)
12. G. Bersuker, J. H. Sim, C. D. Young, R. Choi, P.M. Zeitzoff, G. A. Brown, B. H. Lee, and R. W. Murto, *Microelectron. Reliab.*, **44**, 1509 (2004).
13. G. Mavrou, S. Galata, P. Tsipas, A. Sotiropoulos, Y. Panayiotatos, A. Dimoulas, E. K. Evangelou, J. W. Seo and Ch. Dieker, *J. Appl. Phys.,* **103**, 014506 (2008).
14. E.K. Evangelou, M.S. Rahman, I. I. Androulidakis, A. Dimoulas, G. Mavrou, K.P. Giannakopoulos, D.F. Anagnostopoulos, R. Valicu, G.L. Borchert,, *Thin Solid Films*, **518**(14), 3964 (2010).
15. E.K. Evangelou, M.S. Rahman, and A. Dimoulas, *IEEE Trans. Electron Devices,* **56**(3), 309 (2009).
16. D. M. Fleetwood, *IEEE Trans. Nulc. Sci.*, **39**, 269, (1992)
17. D. M. Fleetwood and N. S. Saks, *J. Appl. Phys.*, **79**, 1583, (1996)
18. D. K. Chen, R. D. Schrimpf, D. M. Fleetwood, K. F. Galloway, S. T. Pantelides, A. Dimoulas, G. Mavrou, A. Sotiropoulos, and Y. Panayiotatos, *IEEE Trans. Nulc. Sci.,* 54, 971 (2007).
19. A. Dimoulas, D.P. Brunco, S. Ferrari, J.W. Seo, Y. Panayiotatos, A. Sotiropoulos, T. Conard, M. Caymax, S. Spiga, M. Fanciulli, Ch. Dieker, E.K. Evangelou, S. Galata, M. Houssa, M.M. Heyns, *Thin Solid Films* **515** 6337 (2007).