Current instabilities in rare-earth oxides-HfO_2 gate stacks grown on germanium based metal-oxide-semiconductor devices due to Maxwell–Wagner instabilities and dielectrics relaxation

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The authors report the current instabilities in rare-earth oxides-HfO_2 gate stacks grown on Ge (001) based metal-oxide-semiconductor devices under constant voltage stress (CVS). The devices have been subjected to CVS and show relaxation effect and charge accumulation/trapping at the interface of the high-*k* bilayers known as Maxwell–Wagner (MW) polarization; both cause current instabilities (i.e., current decay). The experimental data can only be explained when co-occurrent effects of MW instability and dielectric relaxation are taken into consideration. On the contrary, any single effect alone is unable to fit and/or explain the results completely. It is interesting that these effects show field dependent behavior; that is, at low CVS, the authors observe the current instabilities (follow $J \sim t^{-n}$ law), whereas at higher field, the charge trapping and/or the creation of new defects in the oxides, which eventually lead to breakdown, are significant. These results are also confirmed by capacitance-voltage $(C-V_g)$ measurements in respective conditions. © *2011 American Vacuum Society.* [DOI: 10.1116/1.3532946]

I. INTRODUCTION

As germanium offers higher mobility when compared to silicon, it draws an extra attention in the semiconductor industry.[1] Ge is highly reactive with high-*k* HfO_2, and when HfO_2 as a single layer is grown on Ge substrates to form metal-oxide-semiconductor (MOS) devices, it does not show good structural and electrical properties. So, an approach is to use rare-earth oxides (REOs) (e.g., CeO_2, La_2O_3, and Dy_2O_3, etc) dielectrics as an interfacial buffer layer, which are well-disposed with Ge and can also be directly deposited on it, forming a gate stack (with HfO_2) and demonstrates better electrical characteristics as well as passivation properties.[2] As a matter of fact, the reliability characteristics, such as charge accumulation at the interfaces of the two high-*k* dielectrics, charge trapping and defect generation in the bulk of the oxides, stress-induced leakage current (SILC), and oxide degradation, are imperative to understand well before being used as a gate stack. We have observed, initially, that current decay in the gate stacks and it cannot be well explained with charge trapping mechanism in the bulk of the oxides, but this decay behavior describes completely by the simultaneous effects of charge accumulation at the interface of high-*k* bilayer and dielectric relaxation. The gate stacks are the compositions of two different dielectrics and it means that they will also have different conductivities. Thus, charge will accumulate at the interface of dielectrics until, in steady state, the same current density flows through both layers, and this so called Maxwell–Wagner (MW) polarization causes current instabilities.[3] The charge accumulation at the interface of the two layers also stimulates dielectric relaxation effects in each high-*k* layers. Dielectric relaxation is a bulk-related phenomenon that causes relaxation current following the direction of dV/dt.[4] When the applied voltage is low, the transient current is primarily contributed by polarization and the corresponding relaxation. When an external field is applied across a film, it separates the bound charges, thus resulting in polarization and a compensating internal field.[5] Dielectric relaxation is a continual buildup of polarization following the application of an electrical bias, which may be thought of as a time dependent increase in the static (not ac) dielectric constant of the material. Nevertheless, neither of the single mechanisms does fit the experimental data nor explain completely the current decay behavior with stress time which will be more discussed in the experimental results.

Charge trapping precludes accurate extraction of mobility of the devices,[6] and the phenomenon is commonly observed in most of the high-*k* dielectric materials.[7–9] The crucial concern is to understand why and where charge trapping takes place in the bilayers gate stack. It has been widely accepted that the trapped charge resides in localized electronic states associated with structural defects,[9–11] pre-existing bulk

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defects,[6,12] dangling bonds at Ge-semiconductor/dielectric interface,[13] oxygen vacancy, and divacancies,[14] at the interface of two layers of the gate stacks.[3]

The aforementioned effects produce the current instabilities in MOS devices already known, which are contained in various gate dielectrics. They both give a $J_g \sim t^{-n}$ behavior, which is strongly voltage dependent.[3,15] Moreover, these instabilities are usually both present simultaneously, at the same time, making the corresponding analysis a very complex task, and this is the main focus of the present work of the REOs-HfO_2 gate stacks grown on Ge substrates.

II. EXPERIMENT

Gate stacks (e.g., Dy_2O_3/HfO_2, La_2O_3/HfO_2, and CeO_2/HfO_2) films used in the present study were prepared by molecular beam deposition on both *n*-/*p*-type (001) Ge substrates with a resistivity of 1.6–1.9 Ω cm. Prior to deposition, all samples were annealed at 360–400 °C for several minutes until a clear (2×1) reconstruction pattern appeared, indicating a clean Ge surface. The oxides were subsequently deposited at 360 °C (La_2O_3), 225 °C (Dy_2O_3), and 225 °C (CeO_2). As-deposited samples were used for this study. Metal-insulator-semiconductor capacitors by area $A=7\times10^{-4}$ cm^2 were finally fabricated. The thicknesses of the samples were estimated by x-ray reflectivity measurement. The top gate electrode was prepared by e-beam evaporation of 30 nm thick Pt using a shadow mask to define circular dots of 300 μm in diameter, while the back Ohmic contact was realized using eutectic In–Ga alloy. The capacitance-voltage ($C-V_g$), current versus time (J_g-t), and current versus gate voltage (J_g-V_g) characteristics of the MOS capacitors were studied using an Agilent 4284A LCR meter, a Keithley 617 electrometer and appropriate programming, using "stress and sense technique", more details can be found elsewhere.[8] All the measurements were done in a dark box and at room temperature. The maximum variation of temperature during the experiment never exceeded ±0.5 °C. Fresh devices were used for each stress measurement.

III. RESULTS AND DISCUSSION

REOs (La, Ce, Dy, and Gd) are "friendly"[2] with germanium substrates and these form germinates (i.e., RE–Ge–O).[16,17] They react strongly with the substrate resulting in catalytic oxidation of Ge and in the spontaneous formation of stable interfacial layers.[16–19] La_2O_3, CeO_2, Dy_2O_3, and Gd_2O_3 dielectrics have been studied extensively and reported in the literatures.[2,16–19] And one can find, from where the reduced density of states (D_{it}) to 10^{12} cm^{-2} eV^{-1} or below, raising concerns about their scalability to low equivalent oxide thickness values and medium high-*k* values $k\sim9-12$ (Ref. 16), but the leakage current is very high ($V_{FB}\pm1$ V is $\sim$mA/cm^2) (Refs. 8 and 17–19), which is indeed a drawback for MOS devices to use REOs as single dielectric layer. To improve the electrical characteristics, especially to reduce the leakage current, the proposed concept to form gate stacks with high-*k*, such as HfO_2 or ZrO_2 (Refs. 16–19), which could reduce leakage current of the corresponding MOS devices. When REOs act as interfacial layers on the top of Ge (001) substrates, formed gate stacks together with HfO_2 exhibit good electrical and structural characteristics.[16,18,19] The current density versus voltage (J_g-V_g) curves are plotted in Fig. 1(a), where the leakage current properties have been improved, that is, J_g is less than REOs as a single high-*k* dielectric MOS device. We have noticed that the current instability in Dy_2O_3/HfO_2 gate stacks is more pronounced than those of CeO_2/HfO_2 and La_2O_3/HfO_2 stacks, while the leak-

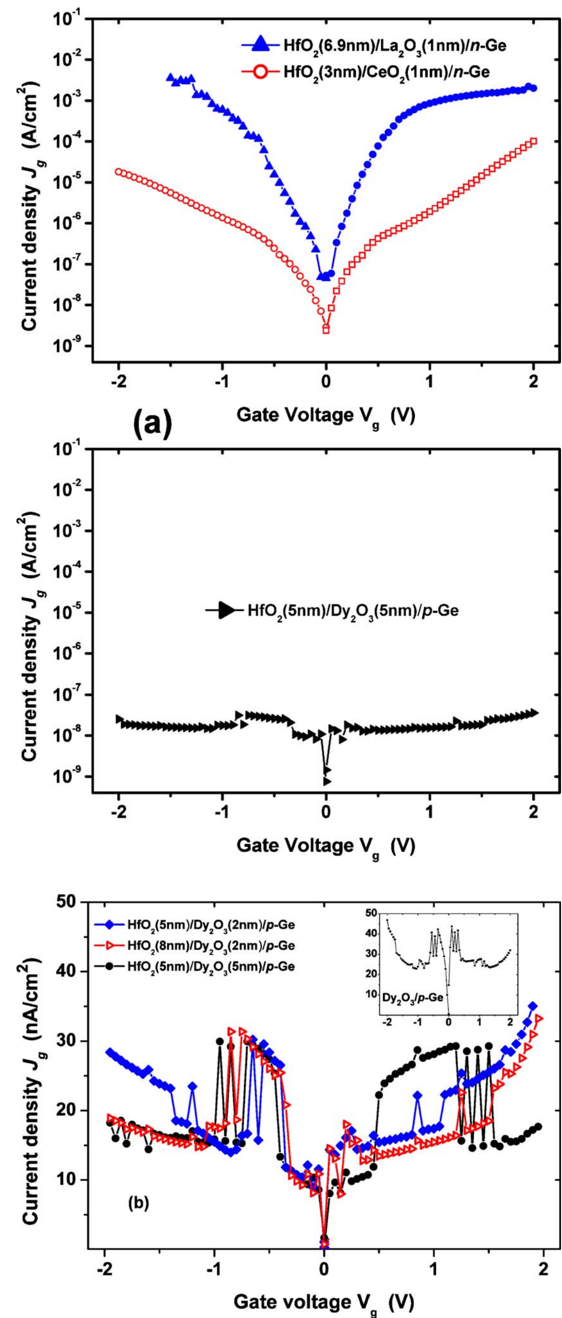

FIG. 1. (Color online) [(a) and (b)] Plot of current density as a function of gate voltage (J_g-V_g) is illustrated in the figure. (a) J_g-V_g characteristics of gate stacks and REOs ($La_2O_3CeO_2Dy_2O_3$)/HfO_2. (b) Typical J_g-V_g characteristics of Dy_2O_3/HfO_2 gate stacks (different compositions) where it is evident that current instabilities are prevailing in both polarities. The inset is the J_g-V_g characteristics of single layer (Dy_2O_3/*p*-Ge) MOS capacitor.

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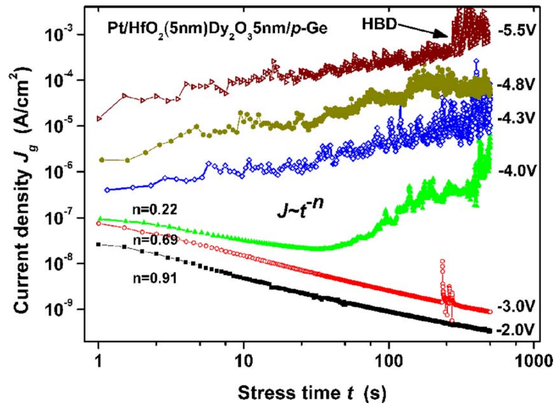

FIG. 2. (Color online) Current transient (J_g-t) behaviors are illustrated at various bias conditions (−2.0 _ −5.5 V) at accumulation of Dy_2O_3(5 nm)/HfO_2(5 nm) gate stacks. At low CVS, current decays are observed, while at higher CVS, the charge tapping and creation of new defects are observed.

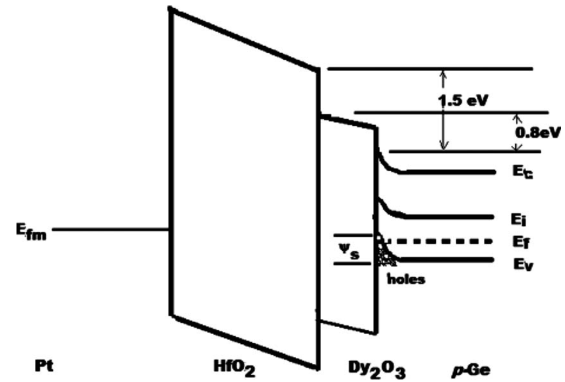

FIG. 3. Illustration of energy band diagram of gate stack (HfO_2/Dy_2O_3) dielectrics under accumulation condition. The conduction band offset between Ge and high-*k* dielectric is 1.5 eV.

age is lower ($V_{FB}\pm1$ V is $\sim$nA/cm^2)[19] than other two stacks,[16,18] which is a sign of good integrity of the corresponding gate stack.[15]

We scan the J_g-V_g characteristics of the Dy_2O_3/HfO_2 gate stacks of different compositions and a decipherable picture of the current instability is observed [as shown in Fig. 1(b)]. This is the typical J_g-V_g curves of the gate stacks; all the capacitors show extremely low leakage currents with a typical value around ~15–24 nA/cm^2 at $V_g=V_{FB}-1$ V. For the case of single Dy_2O_3 layer, it shows slightly higher current density, which can be explained by its smaller bandgap and medium-*k* value, as shown in the inset of Fig. 1(b). Another noticeable feature observed in the J_g-V_g curves is the current instability during the measurement regardless of the applied bias (V_g) polarity.[19] This behavior could be explained by random telegraph signal[20] attributed to charge accumulation at the interfaces of the high-*k* dielectrics[3] or trapping/detrapping effects,[10] which seem to be very interesting for the specific combination of the high-*k* oxides used.

To study the current instabilities of REOs-HfO_2 gate stacks grown on Ge substrates, we applied different constant voltage stress (CVS) bias (from −2 to −5.5 V) on Dy_2O_3/HfO_2 samples to measure current transient (J_g-t) characteristics. The current densities as a function of stress time (J_g-t) curves of the corresponding devices are shown in Fig. 2, and this illustrates the current instabilities at different CVS bias condition. Initially, at low bias, the current decay follows $J_g\sim t^{-n}$ behavior, where n is extracted less than unity (0.2~0.9) (Refs. 21 and 22) meaning it is insufficient to explain the experimental results by charge trapping at the pre-existing traps, but described by dielectric relaxation mechanism. At low CVS, the current decay behavior visible, while at medium and high CVS situations, it is different, that is, charge trapping along with creation of new defects (i.e., SILC), which eventually leads the device to breakdown is ascertained.[21,22] One can explain the results entirely when charge accumulation at interface of the high-*k* dielectrics due to different conductivities of the layers (e.g., HfO_2 and Dy_2O_3) and the dielectric relaxation are in consideration. The energy band diagram of the gate stacks (HfO_2/Dy_2O_3) is shown at the accumulation bias condition in Fig. 3 for different conductivities of the dielectric layers. However, at higher CVS, the dominating mechanism is charge trapping in the bulk of the oxides and SILC,[8,21,22] and more details of these results will be discussed in the following paragraphs.

Figures 4(a)–4(c) represent the current instabilities (J_g-t transient characteristics) of three different REOs/HfO_2 gate stacks. All these capacitors have similar behavior; that is, current decays with the progress of stress time when the devices are under CVS conditions. As there is no apparent source of positive/negative charges when the n/p-Ge MOS devices are biased in accumulation, respectively; one of the realistic explanations is the presence of relaxation effects. These effects are expected to be detected in high-*k* films when the leakage current is very low. Therefore, a typical method for the estimation of the relaxation currents is to be measured after the sudden removal of a constant voltage on the gate. However, this article was focused on the investigation of MW instability, i.e., charge accumulation and current instabilities, and such a measurement was not done. An attempt was made to fit the experimental data (current decay) with the Curie–von Schweidler (CS) relaxation law[23] ($J=C\cdot t^{-n}$, C is a constant)[23] and $n=0.73$ from the fit, which is not unity. Both MW and CS mechanisms are taking place simultaneously in the devices during CVS and this could be a reason for the deviation of n from 1 (unity). Due to the composition of the gate stacks, charges will accumulate at the interface of two high-*k* layers until it reaches to uniform conductivity flows through the both layers, which is also known as MW instability. It is interesting to add that when the MOS capacitor (Dy_2O_3/HfO_2) is under CVS at −2.0 V [Fig. 4(a)] for several successive stresses of 500 s each (total is 5000 s), the n value is gradually increasing with respect to each stress to 0.91 which is very close to unity.[22] This increase of n values can be interpreted as, with the progress of time (CVS duration), the more and more charges accumulate at the interface between two high-*k* bilayers due to the fact that the conductivities are approaching to a steady state. Fi-

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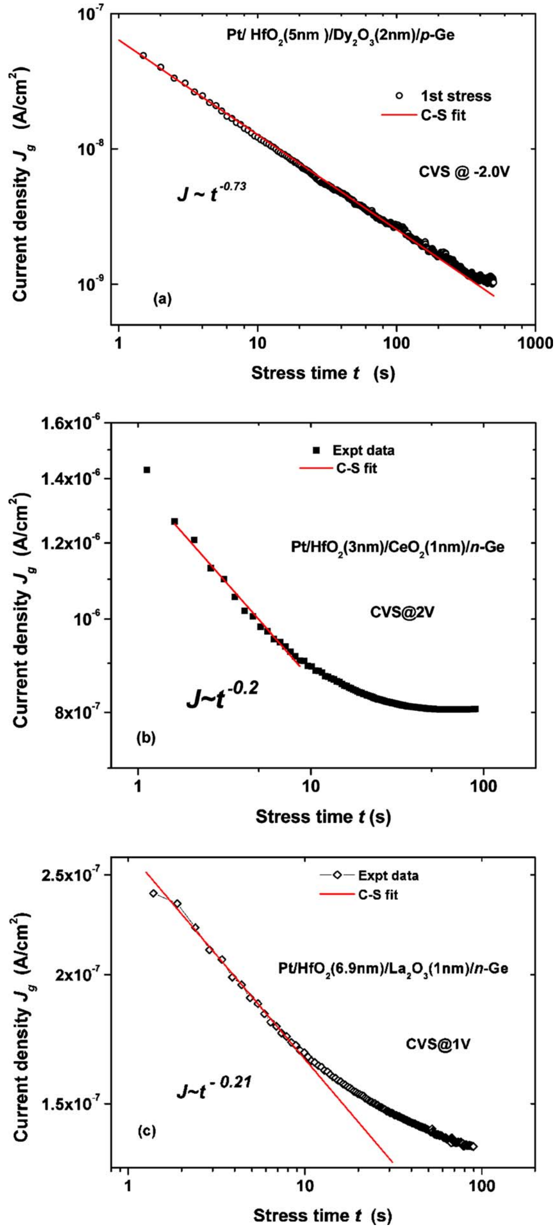

FIG. 4. (Color online) [(a)–(c)] Current decay (instabilities) characteristics of different gate stacks in (a) Dy_2O_3)/HfO_2, (b) CeO_2/HfO_2, and (c) La_2O_3/HfO_2. Solid lines are the fit to experimental data by CS relaxation law.

nally, the MW instability is becoming less important than that of dielectric relaxation; as a result, the n value increases slowly. While the conductivity of the both layers is uniform, the charge accumulation comes to almost in saturation and n tends to unity. CS relaxation is then the dominant process. On the contrary, the relaxation effects are very weak in Figs. 4(b) and 4(c),[23] and the values of n after CS fit are 0.2 and 0.21 at CVS of 2 and 1 V for CeO_2/HfO_2 and La_2O_3/HfO_2 gate stacks, respectively. The n values we have extracted using CS fit are far away from unity, which indicates that the only single CS relaxation mechanism is unable to explain the results completely, but this current decay behavior could be explained with field lowering model.[21]

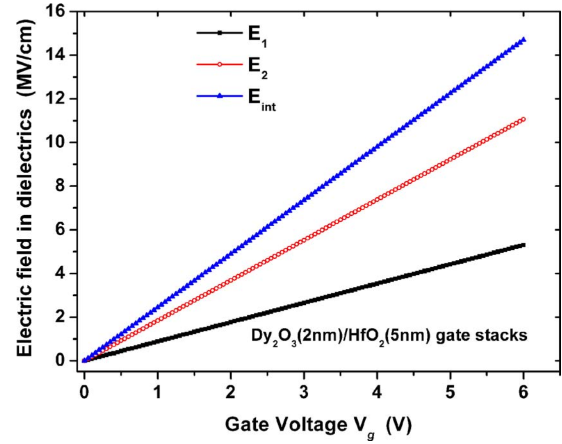

FIG. 5. (Color online) Electric fields ($E_{HfO_2,Dy_2O_3,int}$) across each of the dielectrics vs gate voltage applied (V_g) of the Dy_2O_3/HfO_2 gate stacks.

During the CVS, the important topic is to calculate the correct fields across each of the layers. As we know,[3] the charges are accumulated at the interface between the dielectrics even though the charge trapping is also occurring in the bulk of the oxides, making the task very complex to estimate the exact fields across each of the layers. Apart from the fact, it is also crucial to have an idea or rough estimation of fields when we set the CVS pulse to the devices. From our previous results,[19] we know that when Dy_2O_3 layer is passivated on Ge, it forms an unwanted GeO_2 interfacial layer with Ge. To calculate precise initial electric field across the HfO_2 and Dy_2O_3 films, we have also taken into consideration the interfacial layer forms by it. The field across each of the layers of the gate stacks can be calculated as follows:[24]

$$E_1 = \frac{V_{appl}}{t_1\left[\frac{\kappa_1}{t_l}\left(\left(\frac{t_2}{\kappa_2}+\frac{t_{int}}{\kappa_{int}}\right)+1\right)\right]}, \quad (1)$$

$$E_2 = \frac{V_{appl}}{t_2\left[\frac{\kappa_2}{t_2}\left(\left(\frac{t_1}{\kappa_1}+\frac{t_{int}}{\kappa_{int}}\right)+1\right)\right]}, \quad (2)$$

$$E_{int} = \frac{V_{appl}}{t_{int}\left[\frac{\kappa_{int}}{t_{int}}\left(\left(\frac{t_1}{\kappa_1}+\frac{t_2}{\kappa_2}\right)+1\right)\right]}, \quad (3)$$

where

$$V_{appl} = V_g - V_{FB} - \Psi_s \quad (4)$$

is the voltage applied to the gate dielectric stack, V_g is the gate voltage, V_{FB} is the flatband voltage, and Ψ_s is the initial surface potential of Ge. $t_{1,2,int}$ is the thicknesses of the high-k (HfO_2), buffer layer (Dy_2O_3), and interfacial (GeO_2) layer between Ge substrate and Dy_2O_3, and k_1, k_2, and κ_{int} being their dielectric constants, respectively, whereas $E_{1,2,int}$ is the electric field across each of these dielectric layers (see Fig. 5). It should be pointed out that the calculation of the initial electric field in the high-k film (E_1), as well as the initial field

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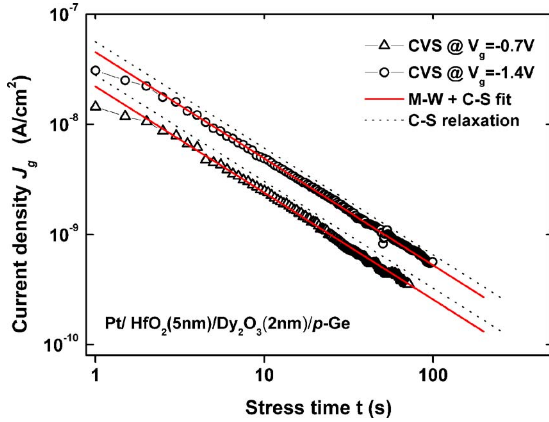


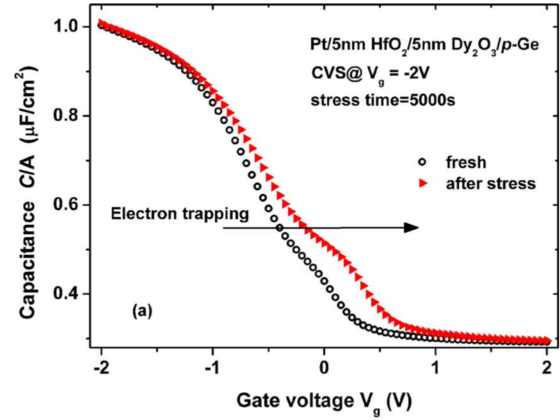
FIG. 6. (Color online) Gate current density as a function of stress time of Dy_2O_3/HfO_2 gate stacks at different low biases (−0.7 and −1.4 V). The solid lines are best fit of Eq. (5) to experimental data. Direct comparison of Fig. 4 shows that the analysis, which is based on the combined effect of CS relaxation and MW instabilities, better describes the observed current decay, while the dotted lines are the fit considering CS relaxation law only. It is worth noting here that the deviation of the experimental data from the linear theoretical line according to Eq. (5) is due to the redistribution of the field across each dielectric (Ref. 3).

across the Dy_2O_3 (E_2), is only an estimation of the magnitudes; these expressions are also valid for two layer dielectrics excluding the third interfacial layer from equations.

If we consider both instabilities are present in the devices during CVS, the relaxation current due to these combined effects (CS and MW instabilities) can be expressed as follows:[3]

$$J_g = \frac{2V_{\text{appl}}\kappa_2\sigma_{0,1}}{t_1\kappa_2 + t_2\kappa_1}\left(3 + \ln\frac{\tau}{\tau_{0,t}}\right)\frac{\tau_{0,1}}{\tau}, \quad \tau > \tau_{0,1}, \tag{5}$$

where τ is the stress time, $\sigma_{0,1}$ and $\tau_{0,1}$ are the material constants that set the scale of current and time, respectively, and other terms are mentioned before. Figure 6 shows the current density as a function of stress time at different low biases of −0.7 and −1.4 V, respectively. We fit the model[3] to the experimental data of HfO_2/Dy_2O_3 gate stacks at two different V_g values using Eq. (5). The thickness of each layer is known from independent measurements, while V, J, and t are experimental data. Nevertheless, we consider two layers gate stacks (HfO_2 and Dy_2O_3) not to go into the complexity of the calculations. As we know,[19] an ultrathin GeO_2 layer is formed between Dy_2O_3 and Ge substrates, which has low k value and that it would have minor effects in the calculation. Therefore, to obtain the values of the free running parameters $\sigma_{0,1}$, $\tau_{0,1}$, and $\kappa_{1,2}$, two sets of experimental $J_g - t$ data were used after the application of different low CVS biases (−0.7 and −1.4 V) on the same sample. From the fit of the experimental data, the relevant parameters have been calculated as $\kappa_1=20$, $\kappa_2=13$, $\sigma_{0,1}=2-3\times10^{-5}$ A/cm², and $\tau_{0,1}=2.1\times10^{-11}$ s, respectively, whereas experimentally κ-values of HfO_2 and Dy_2O_3 are reported to be around $\kappa_1=20-25$ (Ref. 25) and $\kappa_2=12-14$ (Ref. 26), respectively. These values have also been confirmed by means of high frequency $C-V_g$ measurements on similar samples.[19] The dotted lines in Fig. 6 are the fits only with dielectric relaxation (CS) without taking MW effect into consideration, and it is a clear picture that a single mechanism is unable to explain the experimental data completely. It was then reasonable to assume that the current decay was not due to the relaxation effects only. By utilizing the model (see Fig. 6), one can describe that CS relaxation and MW instabilities are acting simultaneously, also note that comparable parameters' values are extracted. One thing to emphasize here is that the instabilities are visible at low and moderate fields/biases, while at higher fields/biases, the situation is different, it shows defect generations and charge trapping behavior.[22] The model of Jameson *et al.*[3] can explain the experimental data of current instabilities for first few seconds but not able to fit the long stress time data at low field.



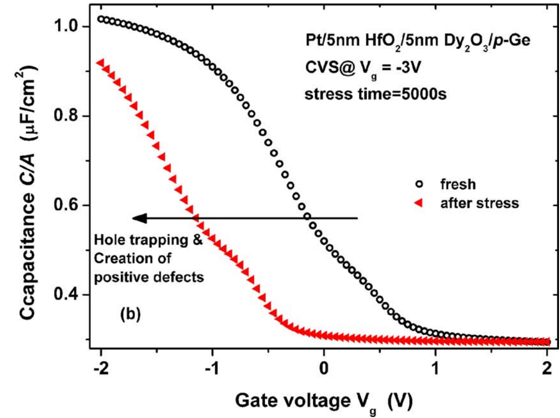


FIG. 7. (Color online) High frequency $C-V_g$ (f=100 kHz) curves on fresh and stressed devices of Dy_2O_3/HfO_2 gate stacks. Only the curve after the application of ten consecutive CVS cycles (500 s each) is plotted for clarity. Stress voltage is low in (a) and moderate in (b). Positive V_{FB} shifts in (a) indicate trapping of electron in the bulk of the oxides, while negative V_{FB} shifts in (b) indicate creation of positively charged defects.

The interesting result comes out from the analysis of high frequency $C-V_g$ curves of Dy_2O_3/HfO_2 gate stacks [as shown in Figs. 7(a) and 7(b)]; when the applied stress voltage is rather low, the trapped charge in the oxide is electrons (i.e., ΔV_{FB} shift is positive), while at moderate stress voltages, the relevant negative shift of the $C-V_g$ curves indicates positive charge trapping or creation of new positive defects.[21,22] The possible explanations of the observed phe-

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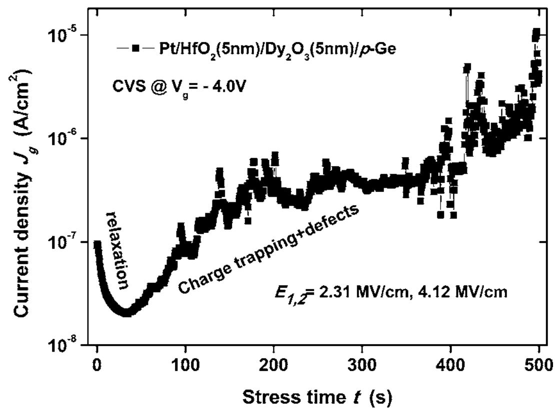

FIG. 8. Absolute J_g vs t, the comparison of the transient current behavior during the application of a stress pulse at a higher gate voltage bias so that the corresponding fields are moderate. Initially, the current decays and then followed by charge trapping behavior that is observed.

nomenon as the gate voltage during the stress pulse is always negative: electrons are injected into the dielectrics from the metal gate. At low voltages, these electrons are trapped in pre-existing defects along with charge accumulation at the interface of the high-k bilayers and the fields across each dielectric are not high enough for these electrons to escape toward the p-Ge substrate. At higher stress voltages, the situation is different, biasing at accumulation, the hole injects from the p-Ge substrate into the oxide and results in the positive charge trapping; also at the same time, a significant amount of new positive defects is created in the bulk of the oxides. Similar behavior (anomalous charge trapping) also observed for the case of $Pt/CeO_2/n$-Ge.[8] We noticed that at low CVS, there was a creation of positive interface defects, while at higher stress field, negative charge trapping occurred at accumulation condition; however, all the biases were in the same polarity even though the current decay behavior was also observed during low CVS bias, which was explained by the trace of relaxation behavior. Usually, CeO_2 behaves like a gate stack composition as this forms germanate (Ce–O–Ge) interfacial layer when deposited on Ge substrates if the dielectric is thick enough (>3 nm).[16,17] For the case of Dy_2O_3/HfO_2 gate stacks (in the present study) and also in $Pt/Dy_2O_3/Ge$ (Ref. 22), results are not shown here; the anomalous ΔV_{FB} shifts have been found at different (low and high) biases, which indicates that the charge trapping along with other mechanisms are present in the devices; however, the CVS bias condition dependency is also illustrated from the results reported.

From Fig. 8, it is very clear that at higher filed (CVS at 4.0 V), the relaxation effects is minor in very few seconds of stress then followed by charge trapping behavior in the bulk of the oxides. At the same time, the creation of new defects illustrates from the figure and the mechanism is gradually dominating. Finally, the device leads to hard breakdown. At moderate CVS, the time dependent $J_g - t$ similar characteristics were illustrated in one of our works on Dy_2O_3/HfO_2 high-k gate stacks.[22] Initially ($t<90$ s), the current decay behavior was found later on with the progress in time; the charge trapping was the main mechanism that was explained by "charge trapping model."[22] Finally, the device followed by the creation of new positive defects decay the current with respect to time, when the critical amount of new defects were created, the device experienced HBD ($>10\,000$ s).

IV. CONCLUSION

Using constant voltage stress pulse, we studied current instabilities such as charge accumulation/trapping and dielectrics relaxation in the rare-earth oxides, REOs/HfO_2 gate stacks grown on Ge (001) substrates. These gate stacks show better electrical properties but the reliability concerns are very important to study explicitly before use as MOS structures. The simultaneous effects, namely, MW instability and CS dielectric relaxation can explicate (fit) the current instabilities (current decay behavior) completely at low bias regime. Nevertheless, any of these single mechanisms alone is unable to fit the experimental data and these phenomena show voltage dependent behavior. At higher field, the charge trapping and new defect generation in the bulk of the oxides are dominant mechanisms. The reliability issues such as charge accumulation/trapping, dielectric relaxation, and defect generation along with other mechanisms in the gate stacks are imperative to study and understand extensively for the gate stacks in MOS devices.

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