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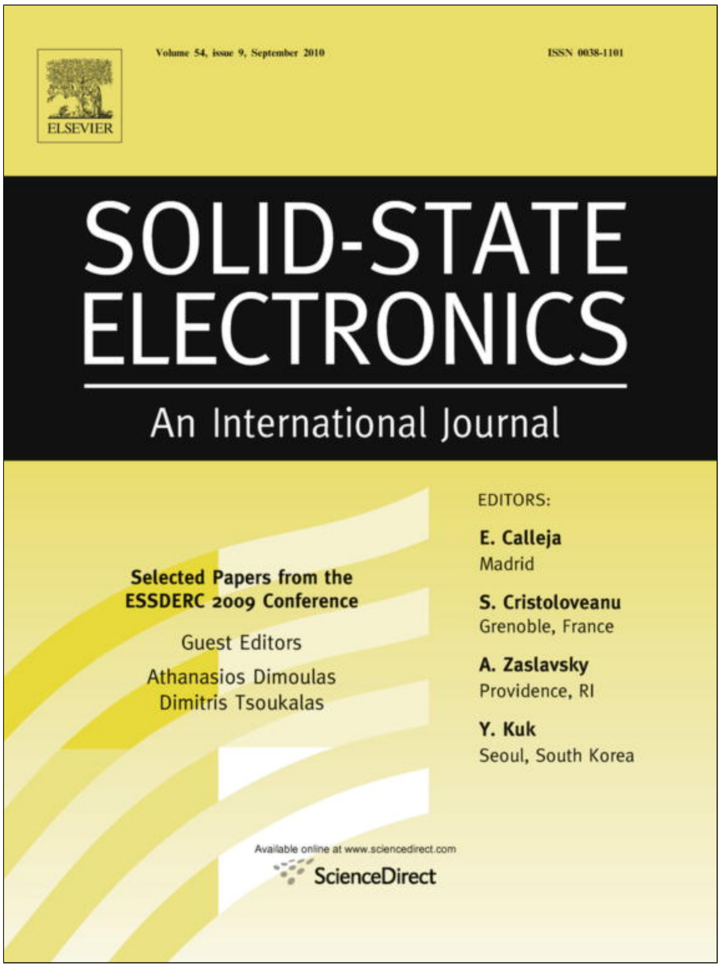
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SILC decay in La_2O_3 gate dielectrics grown on Ge substrates subjected to constant voltage stress

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ABSTRACT

The effect of constant voltage stress (CVS) on Pt/La_2O_3/*n*-Ge MOS devices biased at accumulation is investigated and reported. It is found that the stress induced leakage current (SILC) initially increases due to electron charge trapping on pre-existing bulk oxide defects. After 10 s approximately, a clear decay of SILC commences which follows a t^{-n} power law, with n lying between 0.56 and 0.75. This decay of SILC is not changed or reversed when the stressing voltage stops for short time intervals. The effect is attributed to the creation of new positively charged defects in the oxide because of the applied stressing voltage, while other mechanism such as dielectric relaxation proposed in the past is proved insufficient to explain the experimental data.

Also high frequency capacitance vs. gate voltage (C–V_g) curves measured under different CVS conditions divulge the creation of defects and charge trapping characteristics of La_2O_3 preciously. At low CVS exemplify the generation positively charged defects, however at higher CVS charge trapping obeys a model that was previously proposed and is a continuous distribution of traps.

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1. Introduction

Germanium as a replacement for silicon in future metal–oxide–semiconductor (MOS) technology offers a higher electron (2×) and hole (4×) mobility [1]. However, the critical performance characteristics of MOS capacitors and transistors are determined by the interface between the gate dielectric materials and Ge substrates used. The poor quality of the native oxide (GeO_2) hampered the use of this material in large scale production leaving space for Si/SiO_2 which dominated microelectronics for more than four decades. Rare-earth oxides such as lanthanum oxide (La_2O_3) shows better interfacial and improved electrical characteristics when deposited on germanium substrates resulting the catalytic oxidation of Ge and the spontaneous formation of a stable germanate phase (La–O–Ge) with medium dielectric constant ($\kappa \sim 9$), low density of interface states and good insulating properties [2]. In a recent publication, Houssa et al. [3], suggests that because La is fourfold coordinated in the lanthanum germanate, it produces state-free interfaces with Ge, which could explain the experimentally observed low D_{it} values. Apart from this Ge/oxide interface problem, the reliability concern of the final MOS structure is very important. Various effects such as dielectric relaxation, charge trapping and stress induced leakage currents (SILC), lead to channel mobility and drive current degradation over device operation time.

Charge trapping is a common phenomenon observed in most high-κ dielectric materials [4,5]. During device operation, some charge may be trapped as it passes through the gate dielectric, causing device instabilities such as threshold voltage shifts and drive current degradation [4]. Compared with SiO_2, charge trapping in high-κ materials is much more severe [4,6]. The mechanism of charge trapping is generally believed to be mostly due to trapping on pre-existing defects in the high-κ layer and/or its interfaces.

Stress induced leakage current (SILC) through the gate dielectric of a MOS transistor causes an additional power consumption which is unwanted especially in low power applications; there it may become a reliability issue in those deep-submicron technologies where SILC dominates over the direct-tunneling current [7]. SILC is another limiting factor for down scaling the tunnel oxide thickness in complementary-metal–oxide–semiconductor (CMOS) transistors. It has been widely accepted that SILC path is very localized and measurements on large capacitors can reproducibly reveal the average current density, while a kind of random telegraph signal can be observed on very small capacitors [8]. Additionally, it was reported that SILC is partially due to a transient

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contribution, which decays with time [9], and also this time-decay behavior could be interpreted as the physical mechanism of charge trapping–detrapping from oxide defects [10]. Cester et al. [11] explained the time-decay SILC by two mechanisms, namely, either a local relaxation of the lattice, or a weak spot "clogging" of the oxide neutral defects by injected electrons. It is also widely accepted that the origin of SILC in the bulk of high-κ gate dielectrics is the generation of the neutral oxide traps [12]. When the local trap density reach a critical value, a chain of traps is formed across the, at this time, the current flow become localized and breakdown occurs [13].

Furthermore, another important effect which can influence the performance of MOS devices with high-κ gate oxide is that of dielectric relaxation. It is a bulk-related phenomenon, which causes relaxation current following the direction of dV/dt. Reisinger et al., and Jameson et al., attributed the observed current transients to dielectric material polarization relaxation [14,15], induced by carrier hopping in double potential well. It has been detected in polycrystalline, disordered, or amorphous films but not in single-crystal dielectrics [16]. Dielectric relaxation is a well known and ancient phenomenon, having also been discovered in the 19th century by Curie, and then rediscovered later by von Schweidler. This is now referred to as the "Curie–von Schweidler (CS) law [17]". It is often studied by measuring the transient current that flows in an RC circuit, seems to universally have a time dependence of $1/t^n$, with n slightly less than unity. This time dependence has been observed in various gate dielectric materials such as SiO_2, Si_3N_4, Al_2O_3, ZrO_2, HfO_2, Ta_2O_5, Y_2O_3, perovskites and others. Because dielectric film has very low conductivity, this is a rather slow process [17].

In this paper, we report on the simultaneous effects of charge buildup and SILC decay due to the creation of new bulk defects in La_2O_3 films when the corresponding MOS devices are under constant voltage stress (CVS) condition at accumulation. It is also shown that dielectric relaxation could not explain the experimental results despite of the power law resemblance of the current decay effect.

2. Experimental details

La_2O_3 films presented in this work were prepared by molecular beam deposition (MBD) on n-type (0 0 1) Ge substrates with resistivity of 1.6–1.9 Ω cm. Prior to deposition, all samples were annealed at 360 °C for several minutes until a clear (2 × 1) reconstruction pattern appeared, indicating a clean Ge surface. The oxide was then deposited at 336 °C by evaporating La metal from a Ta effusion cell in the presence of atomic oxygen beams, generated by a remote RF plasma source. The thickness of the La_2O_3 (14.7 nm) was verified by X-ray reflectivity (XRR) and transmission electron microscopy (TEM) measurements. MIS capacitors with area $A = 7 \times 10^{-4}$ cm^2 were then fabricated by e-beam evaporation of 30 nm thick Pt using a shadow mask to define circular dots 300 μm in diameter. The back ohmic contact was eutectic In–Ga alloy. Finally, the sample was subjected to H_2 annealing at 200 °C for 20 min.

The capacitance voltage (C–V_g), current vs. time (J_g–t), and current–gate voltage (J_g–V_g) characteristics of the MOS capacitors were studied using an Agilent 4284A LCR meter, a Keithley 617 electrometer, and appropriate programming. Charge trapping properties were studied by implementing a pulsing technique (also known as "stress and sense"), which is explained in detail elsewhere [5]. The SILC measurement was assessed by applying a CVS at accumulation for a finite period of time, while monitoring the leakage current repeatedly (J_g–t curve). The maximum variation of temperature during the experiment never exceeded ±0.2 °C. Fresh devices were used for each stress measurements. All the measurements were done in a dark box and at room temperature.

3. Experimental results

Typical J_g–V_g characteristics of the fresh devices are plotted in Fig. 1. As can be observed in Fig. 1 the leakage current was found to be around 2×10^{-7} A/cm^2 at $V_{FB} \pm 1$ V both in accumulation and inversion. The transport mechanism through the dielectric is bulk limited and shows trap assisted behavior at higher voltages and temperatures [17,18]. It should be noted that this is superior characteristic compared to other rare-earth dielectrics such as CeO_2 which has high leakage current for the same thickness due to the small energy gap of 3.3 eV [18,19].

The leakage current is an important issue for any high-κ material which could be used as a gate dielectric in nanoscale device. The current transport mechanism and the related reliability issues need to be understood well. Although constant-field scaling rule may be adopted in designing a nanoscale device structure, the high electric field region near the drain region will still cause serious trap generation at the dielectric/silicon interface and charge injection into the gate dielectric [20,21]. It is one of the major sources causing device instabilities and failure of small-sized MOS devices.

Another important parameter is the inhomogeneity of the films due to the polycrystalline nature of the La_2O_3 films as reported earlier [22]. The average curve shown in Fig. 1 could only be obtained for the MOS devices with the smallest gate area $A = 7 \times 10^{-4}$ cm^2, while any bigger in size MOS diodes were usually resulting in considerably higher leakage currents.

Fig. 2 depicts the stress induced changes of the corresponding high frequency (f = 1 MHz) C–V_g curves. The density of the interface states was estimated to be around 2×10^{11} eV^{-1} cm^{-2} [23]. Noticeably, this D_{it} value was not smaller than that obtained for the as deposited films, thus indicating that annealing in H_2 environment does not improve the interface properties significantly. However, it reduces considerably the hysteresis and the dispersion at accumulation effects.

In other words, the annealed samples are expected to be more reliable, hence they were chosen for the present voltage stress studies at high electric field. In Fig. 2 the C–V_g curves of the fresh device were first measured. A positive bias of the device at accumulation region was applied for stress time ranging from 100 s to 1000 s and the C–V_g characteristic was measured again. The total stress time at a certain applied gate bias was 7000 s.

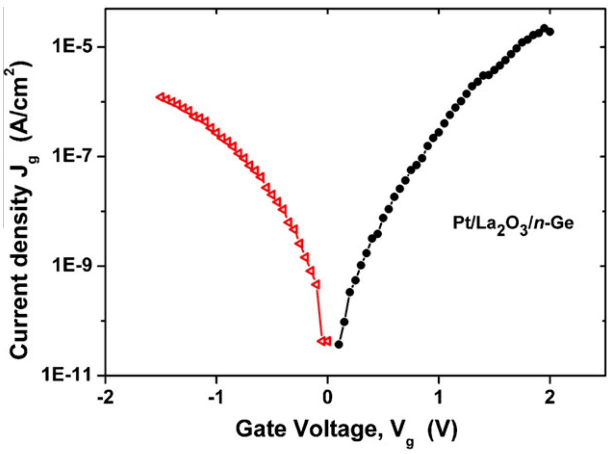

Fig. 1. Density (J_g) vs. gate voltage (V_g) characteristics of Pt/La_2O_3/n-Ge on fresh devices, J_g at $V_{FB} \pm 1$ V is around 2×10^{-7} A/cm^2.

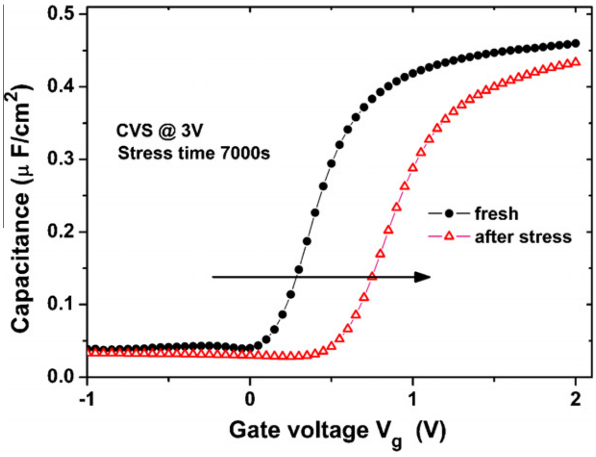

Fig. 2. C–V_g curves before and after 7000 s stress at 3 V during CVS. The V_{FB} shift is positive, hence hinders electron trapping in La_2O_3 dielectrics.

At low CVS (+0.8 V) initially we observe negative charge trapping (positive flatband voltage (V_{FB}) shift) and then after 1000 s approximately – we observe the accumulation of positive oxide charge which could be attributed to the creation of positively charged defects. These defects are so deep that the short time interval needed for the C–V_g acquisition is not enough as to depopulate/wipe-out these defects. Hence after the initial positive V_{FB} shift of the C–V_g's we observe an opposite trend for the shift (V_{FB} shifts towards more negative values).

As shown in Fig. 2 positive CVS at higher gate voltages results in a positive V_{FB} shift of the C–V_g curves due to negative charge trapping in the bulk of the oxide. The observation was confirmed by measuring the J_g–V_g characteristics of the devices subjected to exactly the same CVS conditions but different time intervals.

As explained above, charge trapping together with the creation of new bulk traps act simultaneously and an attempt to describe the law that each mechanism obeys is given below. The dependence of the flatband voltage shift (ΔV_{FB}) on stressing time (t) can be expressed as [5,24],

$$\Delta V_{FB} = \Delta V_{\max}[1 - \exp(-t/\tau)^{\gamma}] \tag{1}$$

where $\Delta V_{\max}$ is the maximum flatband voltage shift, and τ is the time constant of the process. γ is an exponent which characterizes the distribution in capture cross sections. Exponent γ is a measure of the distribution width and its value increases to unity as the distribution width decreases to zero.

The result of various stress fields on the ΔV_{FB} shift is illustrated in Fig. 3a and b, where a positive ΔV_{FB} shift both at low (first 1000 s) and higher bias values is clearly observed. In Fig. 3a the creation of new positive defects (as V_{FB} shifts toward negative (decay) after 1000 s of CVS at + 1 V) follows a power law, that is ΔV_{FB} with respect to t is given by [5,25].

$$\Delta V_{FB} = V_{FB\max} t^{m} \tag{2}$$

The calculated value for $m = 0.74$, lies in the range [0.3–1.0] as reported by many groups in the past irrespective of the substrate material chosen (Si or Ge) [5,26–28]. This behavior has also been observed in our previous reports [5,29] on similar structures (Pt/CeO_2/Ge, Pt/Dy_2O_3/Ge) and is, in general, attributed to the creation of new traps.

In Fig. 3a and b, ΔV_{FB} shifts are positive and they follow the exponential form of Eq. (1). It is interesting to notice that at low CVS conditions (Fig. 3a) the initial (1000 s) experimental data are perfectly fitted by Eq. (1) with $\gamma \approx 1$ [5,24–25]. In this case Eq. (1) describes the filling dynamics of pre-existing bulk oxide traps with no continuous distribution in its capture cross section, while at higher CVS (Fig. 3b) the trap distribution is continuous with the γ value ~0.26 [24,25].

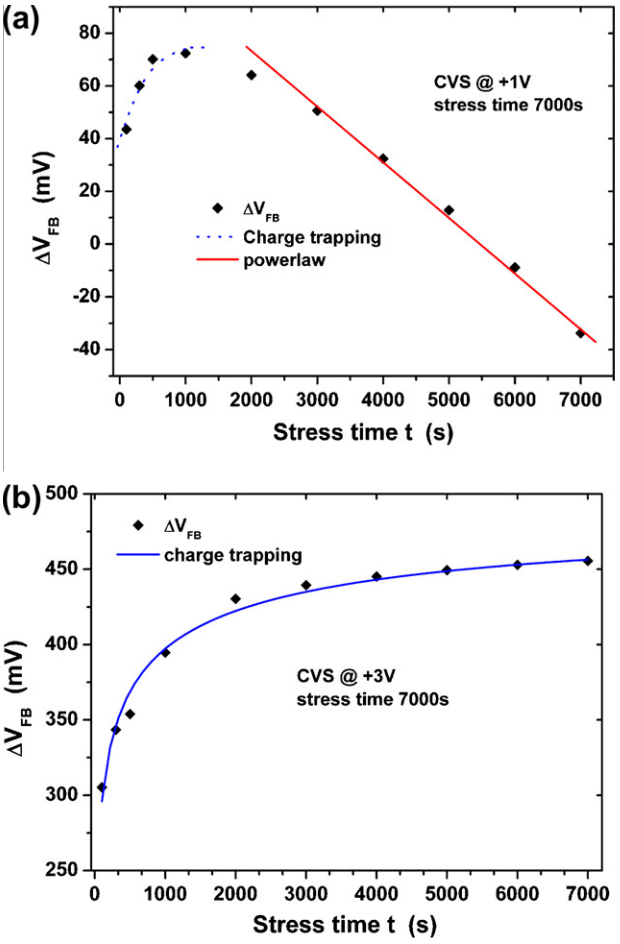

Fig. 3. Flatband voltage shift (ΔV_{FB}) as function of stress time (t) under CVS at (a) +1 V and (b) +3 V. (a) First 1000 s fits a charge trapping model (Eq. (1)) (dotted line) while after 1000 s the generation positive defects follows a power law (Eq. (2)) with $m = 0.74$. (b) Solid line is the fit of charge trapping (Eq. (1)) to the ΔV_{FB} data.

In Fig. 4a the evolution of SILC is vacillating, initially increasing and later on decaying with bias time at low CVS. Fig. 4b shows a clear reduction of the gate current after a total stress time of 7000 s at $V_g = +2$ V. This result can be explained with the effect of electron trapping in the lanthanum oxide which induced a cathode field lowering and hence a reduction in the post-stressed current. In addition, it was found that the amount of trapped charge is proportional to the applied stressing voltage for gate voltages in the range from +0.8 V up to +3 V. The observed decay of SILC [11,28] was then reduced for applied $V_g > 3.0$ V and it was attributed to the fact that the devices show soft breakdown (SBD) and hard breakdown (HBD) phenomena for these applied voltages.

In order to have a clear picture on the charge trapping during stressing, the transient current behavior during the stressing was recorded. Fig. 5a and b shows the current density as a function of time for a number of consecutive CVS cycles at a stress voltage of +2 V.

A large and increasing current is recorded as soon as the first stress cycle commences indicating charge trapping at pre-existing bulk oxide defects. Almost 5 s later the current decays and reaches a constant power law decrease after 100 s approximately. Once each CVS pulse was stopped the J_g–V_g characteristics was sensed for 10 s and then the next voltage pulse was applied. Interestingly,

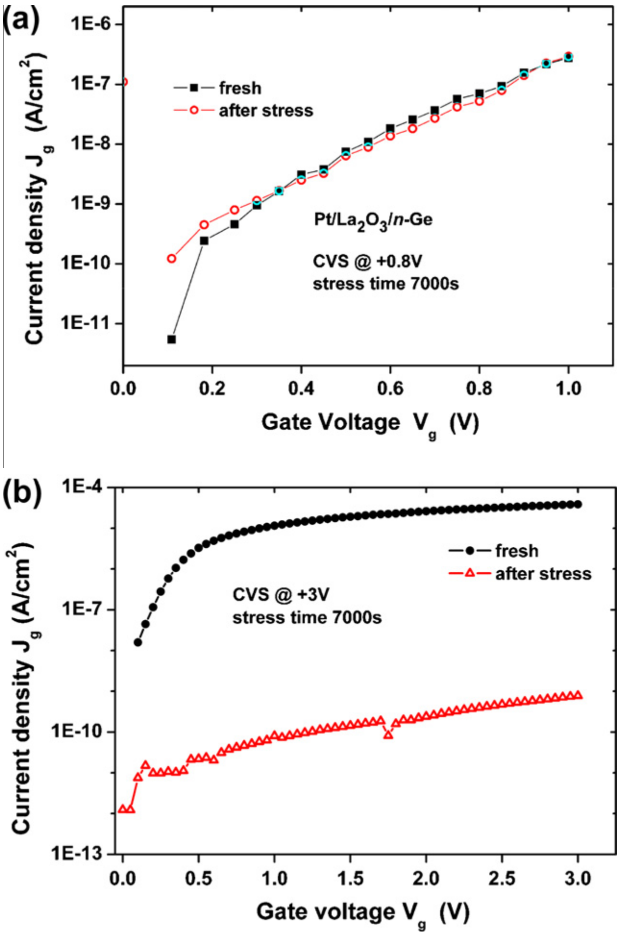

Fig. 4. J_g–V_g characteristics curves on fresh capacitor and after CVS at (a) +0.8 V and (b) +3 V respectively and the SILC decay observed after the stress.

the current during the charge trapping period of the next pulse (0–10 s) never reaches the values of the previous cycle. This is consistent with the electron trapping and the so induced cathode field lowering assumption used to explain the decay of SILC observed in the J_g–V_g curves (Fig. 4b). However, in Fig. 6a collective plot of all J_g–t curves shown in Fig. 5b is given. The first 10 s of each curve other than the first one have been removed in this plot as they are related to charge trapping at pre-existing bulk oxide traps. As can be seen in this plot there is a continuous reduction of the leakage current with the application of a CVS pulse at accumulation, which was not interrupted or cancelled by the 10 s intervals that the gate voltage was stopped for J_g–V_g sense. In other words, upon the application of a CVS pulse at accumulation two effects/processes take place simultaneously: (a) charge trapping of substrate induced electrons on pre-existing bulk oxide traps which saturates after 10 s approximately and (b) generation of new positively charged defects that trap electrons thus resulting in a monotonous decrease of the leakage current following a power law ($\sim t^{-n}$) behavior.

The power n of the latter process is voltage dependent and the devices finally reach breakdown when the amount of bulk defects is so big, that percolation paths start to develop in the oxide. This effect could be observed at higher ($V_g > 4.0$ V) stress voltages when the time-to-breakdown t_{BD} intervals could be easily reached ($t_{BD} \sim 5000$ s in Fig. 7). Similar results have been reported on Al/HfO$_2$/n-Si structures [20] and the authors attribute this power law decrease of the current to merely to the field lowering due to electron trapping. Another experiment showing time-decay of SILC was reported earlier on conventional p-Si based MOS devices with SiO$_2$ as the gate dielectric [11].

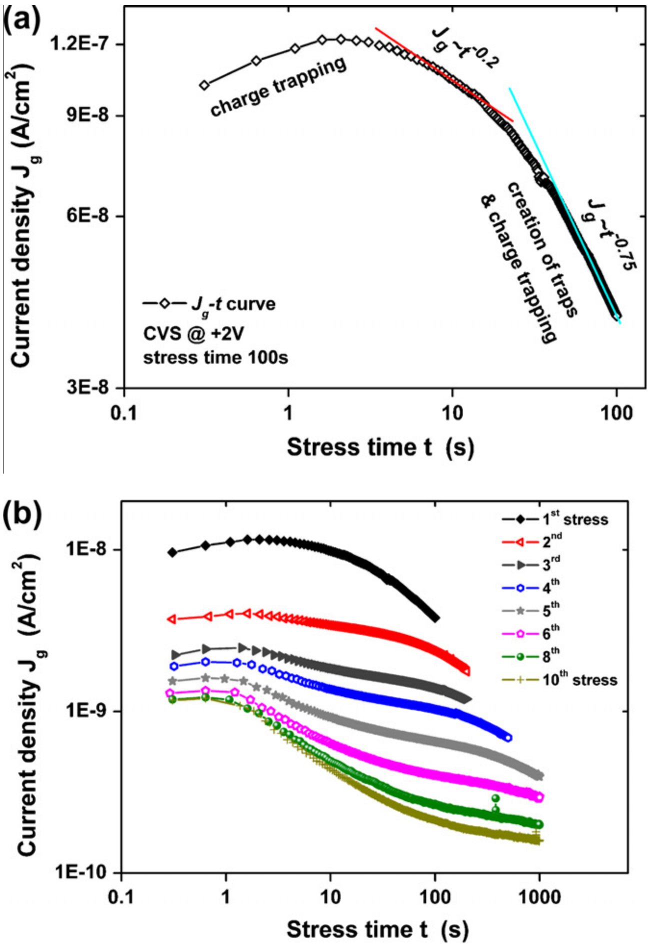

Fig. 5. (a) Current density (J_g) as function of stress time (t) at +2 V during CVS for 100 s on Pt/La$_2$O$_3$/n-Ge capacitor. Initially J_g–t curves shows charge trapping and latter reveals creation of new positive traps. (b) J_g–t successive curves shown on the same device, where the device was stressed for 7000 s.

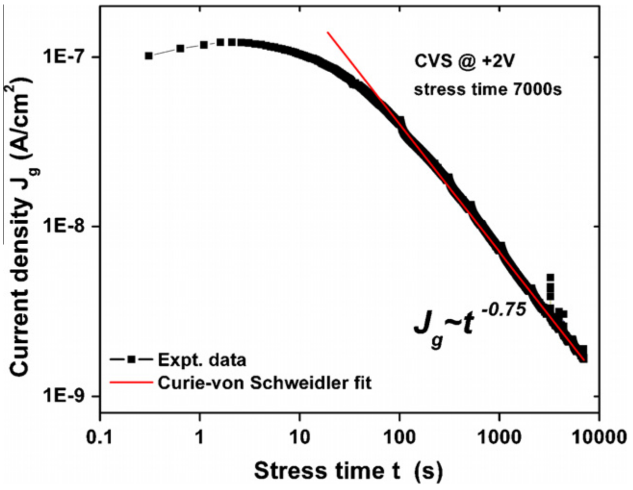

Fig. 6. J_g–t curve at low stress voltage (+2 V) from long time (7000 s) under CVS condition. First 10 s shows charge trapping, i.e. upward curve then current decay is observed, the n value extracted from fit is around 0.75. This could be explain by creation positive traps and field lowering model due to charge trapping in La$_2$O$_3$ dielectrics.

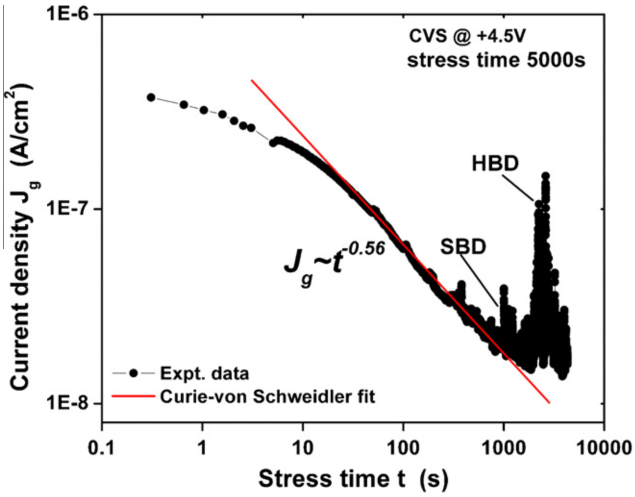

Fig. 7. Current density (J_g) vs. stress time (t) under CVS at higher stress voltage (+4.5 V) for long time (5000 s). The $1/t^n$ fit from experimental data gives n value to be around 0.56, i.e. less than unity, and the creation of critical amount of new trap leads to device SBD and followed by HBD.

The J_g–t results are in complete agreement with those obtained from the study of the C–V_g curves. However, it should be mentioned here that the latter measurements give a clear evidence of the origin of this current decay, i.e. it is the creation of positive charge which is reflected on the relevant V_{FB} shift.

4. Discussions

The nature of SILC in MOS devices has been the subject of a large amount of studies during the last two decades. While a lot of work has been done on Si/SiO$_2$ based structures [11], the complexity of the problem is evident also in more recent MOS devices comprising high-κ gate dielectrics. One of these effects is the decay of SILC with time when the devices are stressed in accumulation. As mentioned in the introduction and experimental sections three different models have been proposed to explain this effect: (a) the field lowering due to electron trapping, (b) "clogging" of the oxide neutral traps and (c) trapping of positive charge in the oxide.

After analyzing our results we propose another mechanism which is based on the previously mentioned models (b) and (c). In particular, immediately after the application of the stressing voltage, trapping at pre-existing defects occurs. Together with this charging effect there is another voltage dependent mechanism which creates positively charged oxide defects. These newly created defects capture more substrate induced electrons thus enhancing the field lowering across the dielectric. In addition, the faster they are created (i.e. the higher the voltage across the dielectric) the more they contribute to a more efficient trap assisted current leakage mechanism thus leading to smaller power n values. Eventually, when the number of bulk oxide defects is so high that percolation paths are easily formed the device goes to breakdown. Moreover, these bulk oxide defects are rather deep and the trapped electrons cannot escape even if the stressing voltage is removed for a long time. It should be mentioned here that in the case of the Si/SiO$_2$ system [11] the authors have shown that the decay rate was continued even when some devices were kept biased at flat band condition for as long as one week between stress and the first SILC measurement.

The simple model of electron trapping and field lowering across the dielectric could be also used to explain the experimental results of the different metal–oxide–semiconductor structures (such as in the present case, in [11] and [20]) where the decay of SILC was found. However, it could not give an answer to the following fundamental questions: (i) why this charge trapping and the corresponding field lowering follow a power law and never reach a saturation point and (ii) why the rate of current decay does not increase continuously with increasing stress voltage (see Figs. 6 and 7).

Another effect which could be claimed as responsible for this decay of SILC is dielectric relaxation. However, the fact that the power n of the t^{-n} dependence for the decay of SILC is far from unity as well as voltage dependence is a very strong argument against this possibility.

Regarding the origin of these bulk defects one could argue that they are nothing more than the well known oxygen vacancies present in most rare-earth oxides. However, the similarity of the results to those reported on conventional poly-Si/SiO$_2$/Si structures may indicate that the creation of H$^+$ species at the oxide/semiconductor interface is also responsible for this deleterious defects generation [26].

5. Conclusions

Pt/La$_2$O$_3$/n-Ge structures have been subjected to CVS at different stress voltages (0.8 to 4.5 V) always at accumulation, and analyzed. The current density of the corresponding fresh device was measured around 2×10^{-7} A/cm^2 at $V_{FB} \pm 1$ V. The positive V_{FB} shift after each CVS cycle indicates the negative charge buildup in the bulk of the oxide during the stress. Also observed is the decrease of the current density during the application of the stressing voltage, which could be attributed to both SILC decay and creation of new positive defects. Initially, the negative charge trapping was more significant mechanism, while later the cathode field lowering model due to charge buildup could explain the current decay. Continuous creation of new positive traps is also another cause of current decay, and their origin could be explicated by the hydrogen release model. Finally, after the creation of a critical amount of defects, the devices reach breakdown.

References

[1] Chen JH, Bojarczuk NAJ, Shang H, Copel M, Hannon JB, Karasinski J, et al. Ultrathin Al$_2$O$_3$ and HfO$_2$ gate dielectrics on surface-nitrided Ge. IEEE Trans Electron Dev 2004;51(9):1441–7.
[2] Mavrou G, Tsipas P, Sotiropoulos A, Galata S, Panayiotatos Y, Dimoulas A, et al. Very high-κ ZrO$_2$ with La$_2$O$_3$ (LaGeO$_x$) passivating interfacial layers on germanium substrates. Appl Phys Lett 2008;93(21):212904.
[3] Houssa M, Pourtois G, Caymax M, Meuris M, Heyns MM. First-principles study of the structural and electronic properties of (1 0 0) Ge/Ge(M)O$_2$ interfaces (M = Al, La, or Hf). Appl Phys Lett 2008;92(24):242101.
[4] Gusev EP, D'Emic CP. Charge detrapping in HfO$_2$ high-κ gate dielectric stacks. Appl Phys Lett 2003;83(25):5223–5.
[5] Rahman MS, Evangelou EK, Dimoulas A, Mavrou G, Galata S. Anomalous charge trapping dynamics in cerium oxide grown on Ge(1 0 0) substrates. J Appl Phys 2008;103:064514.
[6] Evangelou EK, Rahman MS, Dimoulas A. Correlation of charge buildup and stress-induced leakage current in cerium oxides grown on Ge (1 0 0) substrates. IEEE Trans Electron Dev 2009;56(3):399–407.
[7] Blauwe JD, Houdt JV, Wellekens D, Groeseneken G, Maes HE. SILC-related effects in flash E^{2}PROM's-Part II: prediction of steady-state SILC-related disturb characteristics. IEEE Trans Electron Dev 1998;45(8):1751–60.
[8] Tao G, Cop R, Dijkstra J, Kuper F, Verhaar R. The impact of SILC to data retention in sub-half-micron embedded EEPROMs. Microelectron Eng 1999;48(1–4):419–22.
[9] Dunim DJ, Madrix R. Correlation of stress-induced leakage current in thin oxides with trap generation inside the oxides. IEEE Trans Electron Dev 1993;40(5):986–93.
[10] Sakakibara K, Ajika N, Eikyu K, Isikawa K, Miyoshi H. A quantitative analysis of time-decay stress induced leakage current in SiO$_2$ films. IEEE Trans Electron Dev 1997;44(6):1002–7.
[11] Cester A, Paccagnella A, Ghidini G. Time decay of stress induced leakage current in thin gate oxides by low-field electron injection. Solid-State Electron 2001;45:1345–53.
[12] Kimur M, Ohmi T. Conduction mechanism and origin of stress-induced leakage current in thin silicon dioxide films. J Appl Phys 1996;80(11):6360–9.

[13] Degrave R, Groeseneken G, Bellens R, Ogier JL, Depas M, Russel PJ, et al. New insights in the relation between electron trap generation and the statistical properties of oxide breakdown. IEEE Trans Electron Dev 1998;45(4):904–10.

[14] Reisinger H, Steinlesberger G, Jakschik S, Gutsche M, Hecht T, Leonhard M, et al. A comparative study of dielectric relaxation losses in alternative dielectrics. IEDM Technol Dig 2001:12.2.1–4.

[15] Jameson JR, Griffin PB, Agah A, Plummer JD, Kim HS, Taylor DV, et al. Problems with metal oxide high-κ dielectrics due to 1/t dielectric relaxation current in amorphous materials. IEDM Technol Dig 2003:91–4.

[16] Fleming RM, Lang DV, Jones CDW, Steigerwald ML, Murphy DW, Alers GB, et al. Defect dominated charge transport in amorphous Ta_2O_5 thin films. J Appl Phys 2000;88(2):850–62.

[17] Jonscher AK. Dielectric relaxation in solids. J Phys-D: Appl Phys 1999;32:R57–70.

[18] Afanas'ev VV, Shamuilia S, Stesmans A, Dimoulas A, Panayiotatos Y, Sotiropoulos A, et al. Electron energy band alignment at interfaces of (1 0 0) Ge with rare-earth oxide insulators. Appl Phys Lett 2006;88(13):132111.

[19] Rahman MS, Evangelou EK, Androulidakis II, Dimoulas A. Current transport mechanism in high-κ cerium oxides grown on germanium substrates. Electrochem Solid-State Lett 2009;12(5):H165–8.

[20] Zhan N, Poon MC, Wong H, Ng KL, Kok CW. Dielectric breakdown characteristics and interface trapping of hafnium oxide films. Microelectron J 2005;36:29–33.

[21] Wong H, Cheng YC. Generation of interface states at the silicon/oxide interface due to hot electron injection. J Appl Phys 1993;74(12):7364–8.

[22] Mavrou G, Galata SF, Sotiropoulos A, Tsipas P, Panayiotatos Y, Dimoulas A, et al. Germanium metal–insulator–semiconductor capacitors with rare earth La_2O_3 gate dielectric. Microelectron Eng 2007;84:2324–7.

[23] Mavrou G, Galata S, Tsipas P, Sotiropoulos A, Panayiotatos Y, Dimoulas A, et al. Electrical properties of La_2O_3 and HfO_2/La_2O_3 gate dielectrics for germanium metal–oxide–semiconductor devices. J Appl Phys 2008;103:014506.

[24] Zafar S, Callegari A, Gusev E, Fischetti MV. Charge trapping related threshold voltage instabilities in high permittivity gate dielectric stacks. J Appl Phys 2003;93(11):9298–303.

[25] Kumar A, Fischetti MV, Ning TH, Gusev E. Hot-carrier charge trapping and trap generation in HfO_2 and Al_2O_3 field-effect transistors. J Appl Phys 2003;94(3):1728–37.

[26] Houssa M, Steasmans A, Naili M, Heyns MM. Charge trapping in very thin high-permittivity gate dielectric layers. Appl Phys Lett 2000;77(9):1381–3.

[27] Petit C, Zander D. Low voltage stress induced leakage current and time to breakdown in ultra-thin (1.2–2.3 nm) oxides. Microelectron Reliab 2007;47:401–8.

[28] Rahman MS, Evangelou EK, Androulidakis II, Dimoulas A. Study of stress-induced leakage current (SILC) in HfO_2/Dy_2O_3 high-κ gate stacks on germanium. Microelectron Reliab 2009;49(1):26–31.

[29] Rahman MS, Evangelou EK, Androulidakis II, Dimoulas A, Mavrou G, Tsipas P. Investigation of voltage dependent relaxation, charge trapping, and stress induced leakage current effects in HfO_2/Dy_2O_3 gate stacks grown on Ge(1 0 0) substrates. J Vac Sci Technol 2009;B27(1):439–42.