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Defects Generation under Constant Voltage Stress in La_2O_3/HfO_2 Gate Stacks Grown on Ge Substrates

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We report on the defect generation under constant voltage stress in La_2O_3/HfO_2 gate stacks grown on Germanium (001) substrates by molecular beam deposition utilizing a stress and sense technique. A voltage range from 0.5V up to 2.4V was used for the measurements. At low applied gate voltages, the stress induced current decrease could be explained by a field lowering model due to charge trapping, while at higher voltages the generation of shallow traps in the Lanthanum oxide layer becomes more important.

Introduction

Rare-earth (RE) oxides are friendly with Germanium substrates with better passivation properties as an interfacial buffer layer (1). Among the various RE oxides studied La_2O_3 together with HfO_2 as gate stack shows improved electrical properties (2). The reliability of high-κ gate stacks has become one of the most critical factors impacting their introduction in future technology nodes due to the significant progress in high-κ transistor performance (3). A high density of as-grown defects in the transition metal oxides (4) and the presence of a rare-earth oxides (REOs) layer at the interface between the high-κ dielectric and the substrate (1,2,5) complicate the evaluation of stress-induced defect generation in high-κ dielectrics (6,7). Stress induced leakage current (SILC) is another limiting factor for down scaling the tunnel oxide thickness in complementary-metal-oxide-semiconductor (CMOS) transistors. SILC through the gate dielectric of a MOS transistor causes an additional power consumption which is unwanted especially in low power applications; there it may become a reliability issue in those deep-submicron technologies where SILC dominates over the direct- tunnelling current (8). It has been widely accepted that SILC path is much localized and measurements on large capacitors can reproducibly reveal the average current density, while a kind of random telegraph signal can be observed on very small capacitors (9). Additionally, it was reported that SILC is partially due to a transient contribution, which decays with time (10), and also this time-decay behavior could be interpreted as the physical mechanism of charge trapping-detrapping from oxide defects (10,11). Cester, *et. al.*(12) explained the time-decay SILC by two mechanisms, namely, either a local relaxation of the lattice, or a weak spot "clogging" of the oxide neutral defects by injected electrons. It is also widely accepted that the origin of SILC in the bulk of high-κ gate dielectrics is the generation of the neutral oxide traps (13). When the local trap density reach a critical value, a chain of traps is formed across the dielectrics, the current flow become localized and breakdown occurs (14). High- κ dielectrics are trap-rich materials and charge trapping is a common phenomenon observed in most high-κ dielectric materials (15, 16). During device

operation, some charge may be trapped as it passes through the gate dielectric, causing device instabilities such as threshold voltage shifts and drive current degradation (15).

In the present work we report on a number of reliability concerns such as, charge trapping, defects generation and stress-induced leakage current (SILC) of $Pt/HfO_2/La_2O_3/n$-Ge capacitors subjected to constant voltage stress (CVS) conditions.

Experimental

The Hafnium and Lanthanum oxide films used in the present study were prepared by Molecular Beam Deposition (MBD) on *n*-type (001) Ge substrates with a resistivity of 1.6–1.9 Ω-cm. Prior to deposition, all samples were annealed at 360 °C for several minutes until a clear (2x1) reconstruction pattern appeared, indicating a clean Ge surface. The oxides were subsequently deposited at 360 °C. The films have not been post deposition annealed. MIS capacitors with area A=7x10^{-4} cm^2 were finally fabricated. The top gate electrode was prepared by e-beam evaporation of 30-nm-thick Pt using a shadow mask to define circular dots 300 μm in diameter, while the back ohmic contact was realized using eutectic In–Ga alloy.

The capacitance voltage (C–V_g), current versus time (J_g–t), and current versus gate voltage (J_g-V_g) characteristics of the MOS capacitors were studied using an Agilent 4284A LCR meter, a Keithley 617 electrometer, and appropriate programming. Charge-trapping properties were studied by implementing a pulsing technique (also known as "stress and sense"), which is explained in detail elsewhere (16). All the measurements were done in a dark box and at RT. The maximum variation of temperature during the experiment never exceeded ±0.5 ^{o}C. Fresh devices were used for each stress measurement.

Results and Discussion

The electrical characteristics of the MOS capacitors used in the present study have been published in detail elsewhere (2) and only the most important points are summarized here. The Equivalent Oxide thickness (EOT) of the device was around 2 nm, while the density of the interface traps was roughly estimated to be in the low 10^{12} eV^{-1}cn^{-2} range. The as deposited samples showed large hysteresis, stretch-out effects and dispersion both at inversion and accumulation improving only marginally after annealing. It should be mentioned here that single La_2O_3 films grown under similar conditions showed much better electrical characteristics. Hence, the poor quality of the gate stack dielectric is connected with the bilayer structure itself as well as with the quality and stoichiometry of the HfO_2 layer. However, the insulating properties of the bilayer dielectric are significantly improved due to the higher band gap of the top HfO_2 layer used. Fig.1 shows the gate current versus the applied gate voltage (I_g-V) graph. The effect of CVS at accumulation is a clear shift of the I_g-V curve towards higher voltages which can be attributed to an overall lowering of the field across the dielectric due to negative charge trapping on bulk and interface defects.

The effect of CVS at accumulation on the capacitance versus voltage (C-V) curves is illustrated in Figure 2. The electrical stress was applied each time to a fresh devices and the polarity of V_g was chosen so that the device was initially stressed at accumulation (V_g = +2V) and then at inversion (V_g = -2V) for a certain period of time.

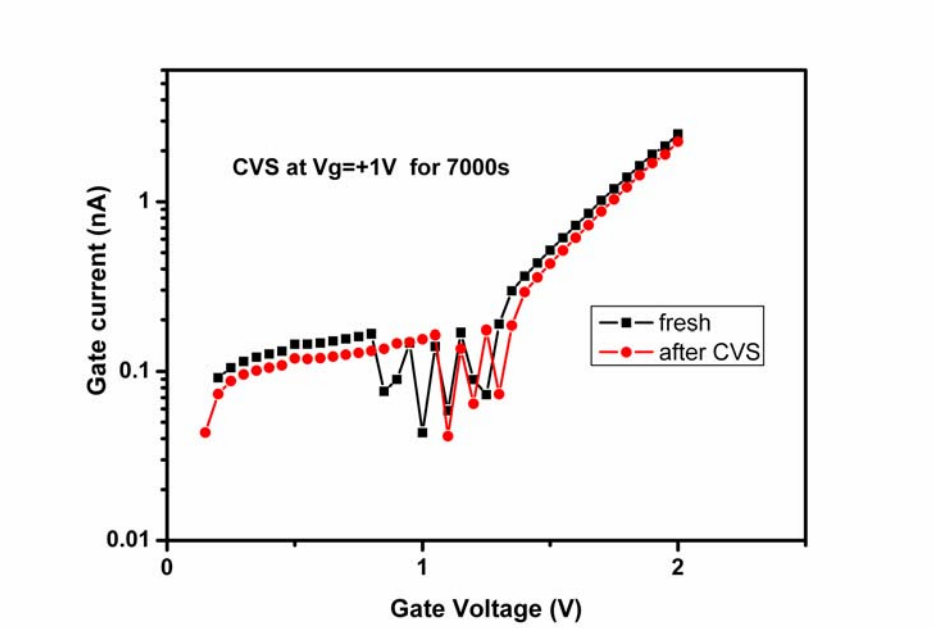

Figure 1. Typical I-V curves of the devices before and after CVS at accumulation.

It should be stressed here that when the device was stress at accumulation, the C-V curve was obtained from accumulation to inversion and backwards so that any charge trapped within the bulk of the oxide layers had no time to escape (detrap). For the fresh devices as well as after CVS at inversion the standard procedure was used (i.e. inversion to accumulation and backwards). As shown in figs. 2a,b the effect of electrical stress is a rather slow process. For stress times shorter than 10s, no detectable change in the C-V could be obtained. However a careful observation of the full hysteresis loop leads to the following qualitative results:

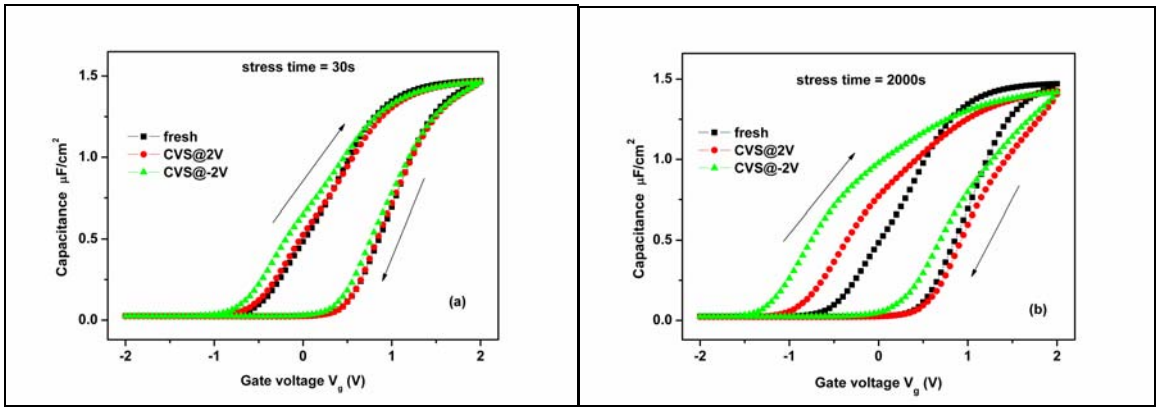

Figure 2. Typical high frequency C-V curves (f=1MHz) of the devices before and after CVS at accumulation or inversion for stress times (a) t_s = 30s and (b) t_s = 2000s. For t_s <10s no change could be observed.

Constant voltage stress at accumulation does not shift the flat band voltage (V_{fb}) significantly. Even when the C-V curve is recorded immediately after the application of

the CVS pulse (red curve in fig. 2a,b), there is no V_{fb} shift. Most high-k materials show the existence positively charged oxide defects. Therefore, by stressing the device at accumulation, a positive V_{fb} shift is expected due to electron charge trapping. In a very nice study of the kinetics of charge trapping in HfO_2 high-κ gate stacks, E.P. Gusev et al. (15, 17) reported on the power dependence of electron trapping with respect to the stressing time.

However, the application of a negative gate voltage (i.e inversion of the MOS capacitor) results in a clear negative shift of V_{fb}. This could only be attributed to a fast detrapping process which leaves the oxide dielectrics positively charged. In addition, it is evident that the application of a CVS pulse either at accumulation or inversion leads to the creation of new positively charged defects. Therefore it is reasonable to assume that during CVS two effects are present simultaneously: (i) the depopulation rate of electrons from the pre-existing bulk oxide defects which is much faster than the corresponding capture rate, and (ii) there is a significant creation of new bulk oxide defects due to the applied electrical stress.

One way to quantify the results obtained from the analysis of the hysteresis loops is by studying the evolution of the so called "border traps" after D. M. Fleetwood (18) who introduced the relative concept in order to describe the oxide traps which are able to exchange charge with the semiconductor substrates on the timescale of the electrical measurements. The effective border trap density, ΔN_{bt} is obtained by measuring a C-V hysteresis curve and integrating the absolute value of the capacitance difference as (19):

$$\Delta N_{bt} \approx (1/qA)\int \left|\left(C_r - C_f\right)\right| dV \qquad [1]$$

where, A is the capacitor area, q the elementary charge, C_r refer to the C-V branch from accumulation to inversion, and C_f refer to the opposite direction.

Experimental data obtained from the C-V curves shown in fig. 2b are shown in figure 3 where $C_{rf} = C_r - C_f$ is plotted against Vg. It is rather obvious that the slower the ramp rate, the more border traps can exchange charge with the Ge substrate. Here a ramp rate of ~0.1 V/s was used, corresponding to switching times of ~40 s over the portion of the curve showing hysteresis. Bulk oxide traps, which do not communicate with Ge on the measurement time scale, are considered here as bulk oxide states, following the common nomenclature of electrical characterisation of MOS devices. From the experimental curves shown in fig.3 it is clear that the application of a CVS pulse either at accumulation or inversion leads to the creation of new border traps with a density proportional to the stress time t_s.

In order to explore the kinetics of electron (de)trapping as well as the creation of new defects during the application of a CVS pulse the gate current was monitored as a function of time. The results are shown in fig. 4 both for (a) low applied CVS voltages and (b) for moderate CVS voltages

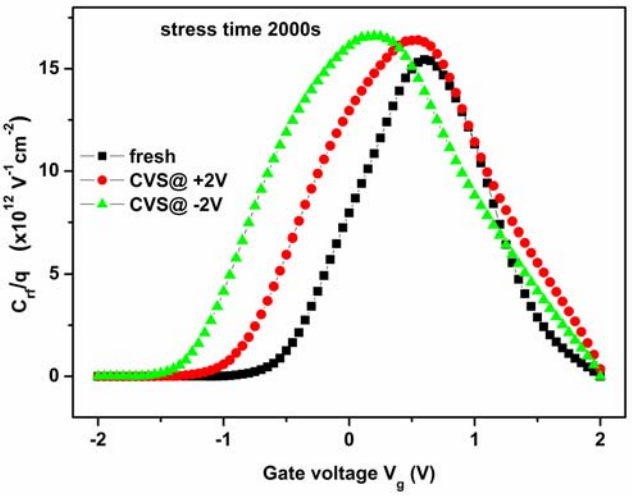

Figure 3. The difference in capacitance between the forward and reverse curves of the C-V characteristics shown in fig. 2b. The area under each curve is proportional to the total number of "border traps" ΔN_{bt} and increases after CVS for t_s=2000s.

In both cases, the current *I* decreases during the application of a CVS pulse at accumulation. However, the effect is more pronounced for lower applied voltages. In this case, the current initially follows a power law ($I \sim t^{-0.7}$) but saturates after 100s approximately. This behavior could be attributed to field lowering due to electron trapping on preexisting bulk oxide traps while there is no indication of trap creation as expected for these low applied stress voltages. However, when the magnitude of the stressing voltage is considerably higher, then the effect of electron trapping is counterbalanced by the creation of new bulk defects which give rise to increasing *I* values with time. Indeed, for even higher CVS values (V_g > 3.5V) a clear increase of the current is observed together with many soft breakdown events which make the corresponding I-t curve rather noisy. Similar results have been observed in Si/SiON/ZrO_2/TiN structures in the past (20) and the authors explained the creation of new defects using the so called "hydrogen release model". In the present case though, the devices have not been annealed

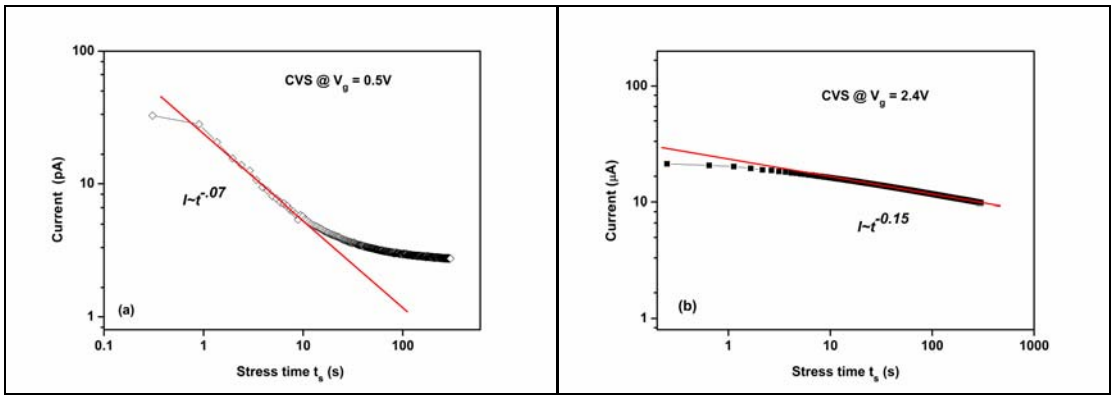

Figure 4. Plots of the current (*I*) as a function of stress time t_s for (a) a low applied stress voltage where *I* decreases significantly, and (b) a moderate stress voltage where *I* decreases only marginally.

in hydrogen hence, the created defects could only be attributed to shallow traps with unknown origin. This is also compatible with the previously analyzed capacitance results. In particular, it is reasonable to assume that the created defects lie close to the La_2O_3/Ge interface (i.e. they are "border traps") and while they can capture electrons during CVS at accumulation (fig.4) they are easily discharged when the applied gate voltage is reversed even for the short period of time that a C-V curve is recorded.

As these results are not consistent with the vast literature on HfO_2 films which suggests that most charges are trapped at deep levels (15-17) we prepared a set of Pt/La_2O_3/nGe structures in order to test the quality of the rare earth oxide buffer layer. Although a detailed analysis of the electrical characteristics and reliability issues regarding these devices will be published elsewhere (21) it is worth mentioning here that the corresponding J-t curves are quite different as illustrated in fig. 5. The major difference is the fact that these devices show a continuous decrease of the current density at accumulation which follows a power law and can be attributed to a stress induced generation of positively charged defects in the bulk of the oxide.

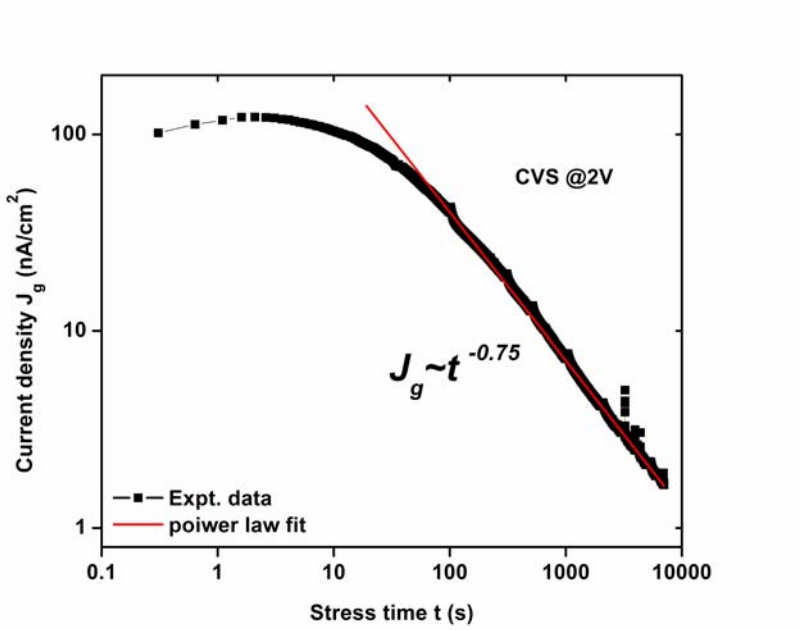

Figure 4. Plot of the current (*I*) as a function of stress time t_s for a moderate applied stress voltage, where *I* decreases monotonously. The dielectric is a single 15nm thick La_2O_3 oxide grown under similar conditions to the other films studied here.

Conclusions

We investigated a number of important issues such as charge trapping-detrapping and defect generation in Pt gated stacks with a thin MBD grown HfO2 high-k layer on top of an ultrathin buffer La_2O_3 layer. Combined capacitance vs voltage and current vs time measurements revealed the existence of a relatively large amount of bulk defects which is enhanced by constant voltage stress induced shallow traps in the La_2O_3 buffer layer.

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