SILC decay in Ge-based MOS devices with La_2O_3 gate dielectrics subjected to constant voltage stress

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***Abstract*—The effect of constant voltage stress on Pt/La_2O_3/n-Ge MOS devices biased at accumulation is investigated and reported. It is found that the stress induced leakage current (SILC) initially increases due to electron charge trapping on pre-existing bulk oxide defects. After 10s approximately, a clear decay of SILC commences which follows a t^n power law, with n lying between 0.56 and 0.75. This decay of SILC is not changed or reversed when the stressing voltage stops for short time intervals. The effect is attributed to the creation of new positively charged defects in the oxide because of the applied stressing voltage, while other mechanisms proposed in the past are proved insufficient to explain the experimental data.**

I. INTRODUCTION

Germanium as a replacement for Silicon in future metal-oxide-semiconductor (MOS) technology offers a higher electron (2χ) and hole (4χ) mobility [1]. However, the critical performance characteristics of MOS capacitors and transistors are determined by the interface between the gate dielectric materials and Ge substrates used. The poor quality of the native oxide (GeO_2) hampered the use of this material in large scale production leaving space for Si/SiO_2 which dominated microelectronics for more than four decades. Rare-earth oxides such as lanthanum oxide (La_2O_3) shows better interfacial and improved electrical characteristics when passivated on Germanium substrates resulting the catalytic oxidation of Ge and the spontaneous formation of a stable germanate phase (La–O–Ge) with medium dielectric constant (κ~9), low density of interface states and good insulating properties[2]. In a recent publication, M. Houssa, *et al.* [3], suggests that because La is fourfold coordinated in the lanthanum germanate, it produces state-free interfaces with Ge, which could explain the experimentally observed low D_{it} values. Apart from this Ge/oxide interface problem, the reliability concern of the final MOS structure is very important. Various effects such as dielectric relaxation, charge trapping and stress induced leakage currents (SILC), lead to channel mobility and drive current degradation over device operation time.

Charge trapping is a common phenomenon observed in most high-κ dielectric materials [4-5]. During device operation, some charge may be trapped as it passes through the gate dielectric, causing device instabilities such as threshold voltage shifts and drive current degradation [4]. Compared with SiO_2, charge trapping in high-κ materials is much more severe [4, 6]. The mechanism of charge trapping is generally believed to be mostly due to trapping on preexisting defects in the high-κ layer and/or its interfaces. As a matter of fact, the use of dielectric layers with higher permittivity should allow us to use thicker films than the equivalent MOS devices with SiO_2, and one would expect to reduce charge trapping and the stress induced leakage current (SILC), thus improving the reliability of the corresponding devices [4].

Stress induced leakage current (SILC) is another limiting factor for down scaling the tunnel oxide thickness in complementary-metal-oxide-semiconductor (CMOS) transistors. SILC through the gate dielectric of a MOS transistor causes an additional power consumption which is unwanted especially in low power applications; there it may become a reliability issue in those deep-submicron technologies where SILC dominates over the direct-tunneling current [7]. It has been widely accepted that SILC path is much localized and measurements on large capacitors can reproducibly reveal the average current density, while a kind of random telegraph signal can be observed on very small capacitors [8]. Additionally, it was reported that SILC is partially due to a transient contribution, which decays with time [9], and also this time-decay behavior could be interpreted as the physical mechanism of charge trapping-detrapping from oxide defects [10]. Cester, *et. al.*[11] explained the time-decay SILC by two mechanisms, namely, either a local relaxation of the lattice, or a weak spot "clogging" of the oxide neutral defects by injected electrons. It is also widely accepted that the origin of SILC in the bulk of high-κ gate dielectrics is the generation of the neutral oxide traps [12]. When the local trap density reach a critical value, a chain of traps is formed across the dielectrics, the current flow become localized and breakdown occurs [13].

Furthermore, another important effect which can influence the performance of MOS devices with high-κ gate oxide is that of dielectric relaxation. It is a bulk-related phenomenon, which causes current relaxation following the direction of dV/dt. Reisinger *et al.*, and Jameson *et al.*, attributed the observed current transients to dielectric material polarization/relaxation [14-15], induced by carrier hopping in double potential wells. It has been detected in polycrystalline, disordered, or amorphous films but not in single-crystal dielectrics [16]. Dielectric relaxation is a well-known and ancient phenomenon, having also been discovered in the 19th century by Curie, and then rediscovered later by von Schweidler. This is now referred to as the "Curie–von Schweidler (CS) law [17]". It is often studied by measuring the transient current that flows in an RC circuit, seems to universally have a time dependence of $1/t^n$, with n slightly less than 1. This time dependence has been observed in various gate dielectric materials such as SiO_2, Si_3N_4, Al_2O_3, ZrO_2, HfO_2, Ta_2O_5, Y_2O_3, perovskites and others. Because dielectric film has a very low conductivity, this is a rather slow process [17].

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In this paper, we report on the simultaneous effects of charge buildup and SILC decay due to the creation of new bulk defects in La_2O_3 films when the corresponding MOS devices are under constant voltage stress (CVS) condition at accumulation. It is also shown that dielectric relaxation could not explain the experimental results despite of the power law resemblance of the current decay effect.

II. EXPERIMENTAL

La_2O_3 films presented in this work were prepared by MBE on *n*-type (001) Ge substrates with resistivity of 1.6–1.9 Ω-cm. Prior to deposition, all samples were annealed at 360 °C for several minutes until a clear (2×1) reconstruction pattern appeared, indicating a clean Ge surface. The oxide was then deposited at 336 °C by evaporating La metal from a Ta effusion cell in the presence of atomic oxygen beams, generated by a remote RF plasma source. The thickness of the La_2O_3 (14.7 nm) was verified by x-ray reflectivity and transmission electron microscopy (TEM) measurements. MIS capacitors with area $A=7\times10^{-4}$ cm^2 were then fabricated by e-beam evaporation of 30-nm-thick Pt using a shadow mask to define circular dots 300 μm in diameter. The back ohmic contact was eutectic In–Ga alloy. Finally, the sample was subjected to H_2 annealing at 200 °C for 20 min.

The capacitance voltage (C–V_g), current versus time (J_g–t), and current-gate voltage (J_g-V_g) characteristics of the MOS capacitors were studied using an Agilent 4284A LCR meter, a Keithley 617 electrometer, and appropriate programming. Charge-trapping properties were studied by implementing a pulsing technique (also known as "stress and sense"), which is explained in detail elsewhere [5]. The SILC measurement was assessed by applying a CVS at accumulation for a finite period of time, while monitoring the leakage current repeatedly (J_g–t curve). All the measurements were done in a dark box and at RT. The maximum variation of temperature during the experiment never exceeded ±0.2 ◦C. Fresh devices were used for each stress measurements.

III. EXPERIMENTAL RESULTS

Typical J_g-V_g characteristics of the fresh devices are plotted in Fig.1. As can be observed in Fig. 1 the leakage current was found to be around 2×10^{-7} A/cm^2 at 1V both in accumulation and inversion. The transport mechanism through the dielectric is bulk limited and shows trap assisted behavior at higher voltages and temperatures [18]. It should be noted that this is superior characteristic compared to other rare-earth dielectrics such as CeO_2 which has high leakage current for the same thickness due to the small energy gap of 3.3 eV [6, 18].

The leakage current is an important issue for any high-κ material which could be used as a gate dielectric in nanoscale device. The current transport mechanism and the related reliability issues need to be understood well. Although constant-field scaling rule may be adopted in designing a nanoscale device structure, the high electric field region near the drain region will still cause serious trap generation at the dielectric/silicon interface and charge injection into the gate dielectric [19-20]. It is one of the major sources causing device instabilities and failure of small-sized MOS devices.

Another important parameter is the inhomogeneity of the films due to the polycrystalline nature of the La_2O_3 films as reported earlier [21]. The average curve shown in Fig.1 could only be obtained for the MOS devices with the smallest gate area $A=7\times10^{-4}$ cm^2, while any bigger in size MOS diodes were usually resulting in considerably higher leakage currents.

Fig. 2 depicts the stress-induced changes of the corresponding high frequency (f= 1 MHz) C-V_g curves. The density of the interface states was estimated to be around 2×10^{11} eV^{-1} cm^{-2}[22]. Noticeably, this D_{it} value was not smaller than that obtained for the as deposited films, thus indicating that annealing in H_2 environment does not improve the interface properties significantly. However, it reduces considerably hysteresis as well as dispersion at accumulation.

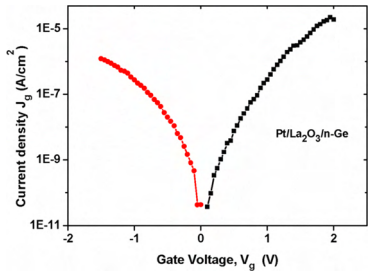

Fig.1. *Current density (J_g) vs. gate voltage (V_g) characteristics of Pt/La_2O_3/n-Ge on fresh devices, J_g at V_{FB}±1V is around 2×10^{-7}A/cm^2.*

In other words, the annealed samples are expected to be more reliable, hence they were chosen for the present voltage stress studies at high electric field. In Fig.2 the C–V curves of the fresh device were first measured. A positive bias of the device at accumulation region was applied for 100 s and then the C–V characteristic was measured again. The same cycle with different stress time was repeated 10 times for a total stress time of 7000 s. As shown in Fig. 2, positive CVS results in a parallel shift of the C-V curves due to negative charge trapping in the bulk of the oxide. The observation was confirmed by measuring the I-V characteristics of

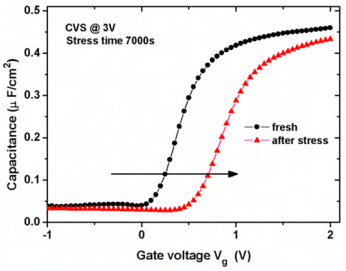

Fig. 2. *C-V curves before and after 7000s stress at 3V during CVS. The V_{FB} shift is positive, hence hinders electron trapping in La_2O_3 dielectrics.*

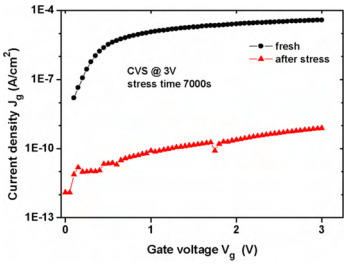

Fig. 3. *Jg-Vg* characteristics curves on fresh capacitor and after CVS at 3V and the SILC decay observed after the stress.

the devices subjected to exactly the same CVS conditions but different time intervals. Fig. 3 shows a clear reduction of the gate current after a total stress time of 7000 s at V_g=+2 V. This result can be explained with the effect of electron trapping in the lanthanum oxide which induced a cathode field lowering and hence a reduction in the post-stressed current. In addition, it was found that the amount of trapped charge is proportional to the applied stressing voltage for gate voltages in the range from +1V up to +3V. The observed decay of SILC [11, 23] was then reduced for applied V_g>3.0V and it was attributed to the fact that the devices show soft breakdown (SBD) and hard breakdown (HBD) phenomena for these applied voltages.

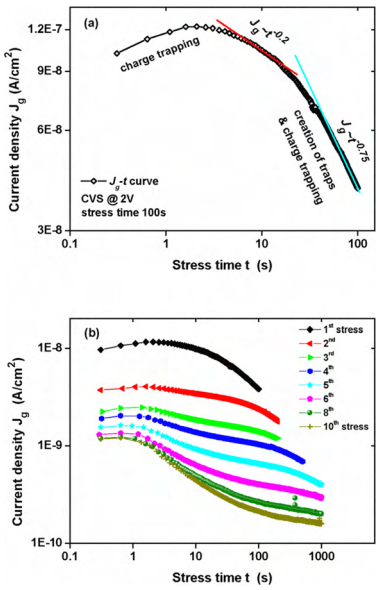

Fig. 4. *(a) Current density (J_g) as function of stress time (t) at 2V during CVS fro 100s on Pt/La2O3/n-Ge capacitor. Initially J_g-t curves shows charge trapping and latter reveals creation of new positive traps. (b) J_g-t successive curves shown on the same device for a total stress time of 7000s.*

In order to have a clearer picture on the charge trapping during stressing, the transient current behavior during the stressing was recorded. Figs. 4(a) and (b) show the current as a function of time for a number of consecutive CVS cycles at a stress voltage of +2V. A large and increasing current is recorded as soon as the first stress cycle commences indicating charge trapping at pre-existing bulk oxide defects. Almost 5s later the current decays and reaches a constant power law decrease after 100s approximately. Once each CVS pulse was stopped the J_g-V_g characteristics was sensed for 10s and then the next voltage pulse was applied. Interestingly, the current during the charge trapping period of the next pulse (0 to 10s) never reaches the values of the previous cycle. This is consistent with the electron trapping and the so induced cathode field lowering assumption used to explain the decay of SILC observed in the J_g-V_g curves (Fig. 3). However, in Fig. 5 a collective plot of all J_g-t curves shown in Fig. 4(b) is given. The first 10s of each curve other than the first one have been removed in this plot as they are related to charge trapping at preexisting bulk oxide traps. As can be seen in this plot there is a continuous reduction of the leakage current with the application of a CVS pulse at accumulation, which was not interrupted or canceled by the 10s intervals that the gate voltage was stopped for J_g-V_g sense. In other words, upon the application of a CVS pulse at accumulation two effects/processes take place simultaneously: a) charge trapping of substrate induced electrons on pre-existing bulk oxide traps which saturates after 10s approximately and b) generation of new positively charged defects that trap electrons thus resulting in a monotonous decrease of the leakage current following a power law ($\sim t^{-n}$) behavior.

The power n of the latter process is voltage dependent and the devices finally reach breakdown when the amount of bulk defects is so big, that percolation paths start to develop in the oxide. This effect could be observed at higher (V_g >4.0V) stress voltages when the time-to-breakdown t_{BD} intervals could be easily reached (t_{BD} ~ 5000s in Fig. 6). Similar results have been reported on Al/HfO_2/n-Si structures [19] and the authors attribute this power law decrease of the current to merely to the field lowering due to electron trapping. Another experiment showing time decay of SILC was reported earlier on conventional p-Si based MOS devices with SiO_2 as the gate dielectric [11]. In this work the authors report on results very similar to those presented here as they have shown that the decay rate was continued even when some devices were kept biased at flat band condition for as long as one week between stress and the first SILC measurement.

IV. DISCUSSION

The nature of SILC in MOS devices has been the subject of a large amount of studies during the last two decades. While a lot of work has been done on Si/SiO_2 based structures [11], the complexity of the problem is evident also in more recent MOS devices comprising high-κ gate dielectrics. One of these effects is the decay of SILC with time when the devices are stressed in accumulation. As mentioned in the introduction and experimental sections three different models have been proposed to explain this effect: (a) the field lowering due to electron trapping, (b) "clogging" of the oxide neutral traps and (c) trapping of positive charge in the oxide.

After analyzing our results we propose another mechanism which is based on the previously mentioned models (b) and (c). In particular, initially after the application of the stressing voltage, trapping at pre-existing defects occurs. Together with this charging effect there is another voltage dependent mechanism which creates positively charged oxide defects. These newly created defects capture more substrate induced electrons thus enhancing the field lowering across the dielectric. In addition the faster they are created (i.e. the higher the voltage across the dielectric) the more they contribute to a more efficient trap assisted current leakage mechanism thus leading to smaller power n values. Eventually, when the number of bulk oxide defects is so high that percolation paths are easily formed the device goes to breakdown. Moreover, these bulk oxide defects are rather deep and the trapped electrons can not escape even if the stressing voltage is removed for a long

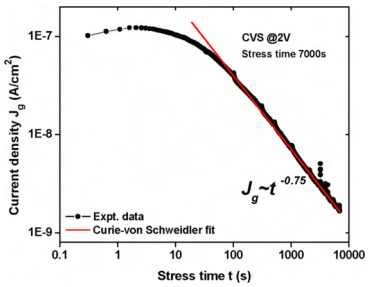

Fig.5*. J_g-t curve at low stress voltage (2V) from long time (7000s) under CVS condition. First 10s shows charge trapping, i.e. upward curve then current decay is observed, the n value extracted from fit is around 0.75. This could be explain by creation positive traps & filed lowering model due to charge trapping in La_2O_3dielectrics.*

time. It should be mentioned here that in the case of the Si/SiO_2 system [11] the authors have shown that the decay rate was continued even when some devices were kept biased at flat band condition for as long as one week between stress and the first SILC measurement.

The simple model of electron trapping and field lowering across the dielectric could be also used to explain the experimental results of the different metal-oxide-semiconductor structures (such as in the present case, in [11] and [19]) where the decay of SILC was found.

However, it could not give an answer to the following fundamental questions: (i) why this charge trapping and the corresponding field lowering follow a power law and never reach a saturation point and (ii) why the rate of current decay does not increase continuously with increasing stress voltage (see Figs. 5 and 6).

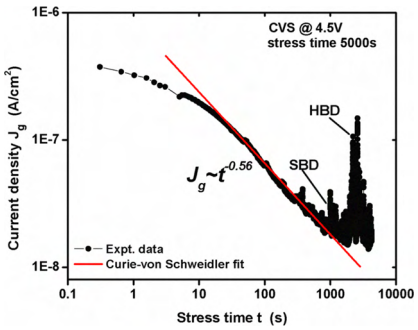

Fig. 6. *Current density (J_g) vs. stress time (t) under CVS at higher stress voltage (4.5V) for long time (5000s). The $1/t^n$ fit from experimental data gives n value to be around 0.56, i.e. less than unity, and the creation of critical amount of new trap leads to device SBD and followed by HBD.*

Another effect which could be claimed as responsible for this decay of SILC is dielectric relaxation. However, the fact that the power n of the t^{-n} dependence for the decay of SILC is far from unity as well as voltage dependence is a very strong argument against this possibility. Nevertheless, it could be even so that, the relaxation is not only one dominant mechanism but also simulations effects of charge trapping and creation of positive traps together, so that n less than unity.

Regarding the origin of these bulk defects one could argue that they are nothing more than the well known oxygen vacancies present in most rare earth oxides. However, the similarity of the results to those reported on conventional poly-Si/SiO_2/Si structures may indicate that the creation of H^+ species at the oxide/semiconductor interface is also responsible for this deleterious defects generation.

V. CONCLUSIONS

Pt/La_2O_3/*n*-Ge structures have been subjected to CVS at different stress voltages (+1V to + 4.5V) always at accumulation, and analyzed. The current density of the corresponding fresh device was measured around 2×10^{-7} A/cm^2 at V_{FB}±1V. The positive V_{FB} shift after each CVS cycle indicates the negative charge buildup in the bulk of the oxide during the stress. Also observed is the decrease of the current density (J_g) during the application of the stressing voltage, which could be attributed to both SILC decay and creation of new positive defects. Initially, the negative charge trapping was more significant mechanism, while later the cathode field lowering model due to charge buildup could explain the current decay. Continuous creation of new positive traps is also another cause of current decay, and their origin could be explicated by the hydrogen release model. Finally, after the creation of a critical amount of defects, the devices reach breakdown.

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