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Current Transport Mechanism in High-κ Cerium Oxide Gate Dielectrics Grown on Germanium Substrates

M. S. Rahman,[a,*] E. K. Evangelou,[a,z] I. I. Androulidakis,[a] and A. Dimoulas[b]

[a]*Laboratory of Electronics-Telecommunications and Applications, Department of Physics, University of Ioannina, 45110 Greece*
[b]*MBE Laboratory, National Center for Scientific Research, Demokritos, Athens 15310, Greece*

The current transport mechanism of Pt/CeO_2/p-Ge metal-oxide-semiconductor devices is investigated. The results are based on the analyses of gate current vs gate voltage curves at temperatures ranging from 295 to 375 K. At low to medium electric fields (~0.1 to 0.9 MV/cm) the main current conduction mechanism is Schottky emission, while Poole–Frankel conduction is the dominant mechanism at higher fields across the oxide (~1.2 to 2.1 MV/cm). The barrier height (Φ_b) at the Pt/CeO_2 interface is found to be equal to 0.91 ± 0.02 eV, while the trap energy level (Φ_t) responsible for the Poole–Frenkel conduction is estimated to be around 0.60 ± 0.03 eV.
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High-κ dielectrics as an alternative to conventional SiO_2 gate oxides are widely investigated for their capability to reduce excessive leakage current in future complementary-metal-oxide-semiconductor (MOS) devices. Although their functionality is already proven and the first integrated devices are in production, further scaling becomes increasingly difficult. Hence, Ge, which offers higher electron and hole mobility than Si, is currently considered as a potential alternative to the standard Si-based MOS technology because it might increase the high-frequency performance of logic devices while keeping the power consumption low.[1] Among the high-κ dielectrics being studied, rare-earth oxides (REOs) are widely investigated because of their interesting structural and electrical properties as a buffer layer on Ge substrates.[2] REOs offer good passivation of Ge, thus reducing the density of interface states (D_{it}), they have reasonably high dielectric constants, and some of them are good insulators with an energy bandgap greater than 5.0 eV.[3,4] In particular, cerium oxide (CeO_2) seems to be an interesting dielectric, because it can be deposited directly on Ge with good thermal stability and improved electrical characteristics such as high dielectric constant ($\kappa \approx 23$)[3] and low interface traps density ($D_{it} \approx 5 \times 10^{11}$ eV/cm^2).[2,5] The moderate bandgap (3.3 eV),[6] together with the small conduction-band offset,[4] lead to relatively high leakage currents ($\sim 10^{-4}$ A/cm^2),[2,4,7] which is a serious drawback if the material is to be used alone and not in a gate-stack configuration.[8]

Recently, Chiu reported on the current conduction mechanisms of CeO_2 deposited on Si(100) wafers with Al as the gate electrode.[9] The author found that Schottky emission is the dominant conduction mechanism in a medium electric field, while Poole–Frenkel emission prevails at higher electric fields and higher temperatures (up to 500 K). In this article, we report on the temperature-dependent carrier transport mechanism of thin (~7 nm) CeO_2 films grown by molecular beam deposition (MBD) and the related energy band diagram of Pt/CeO_2/p-Ge structures.

Experimental

The CeO_2 films studied in the present work were prepared by MBD on p-type (001) Ge substrates with a resistivity of 1.6–1.9 Ω cm. The oxide was deposited at 225°C by evaporating Ce metal in the presence of atomic oxygen beams generated by a radio frequency (rf) plasma source. Metal-insulator-semiconductor capacitors with area $A = 7 \times 10^{-4}$ cm^2 were defined by E-beam evaporation of 30 nm thick Pt using a shadow mask to define circular dots 300 μm in diameter. The thickness of the samples was estimated by X-ray reflectivity measurements to be approximately 7 nm. The electrical properties capacitance–voltage (*C-V*) and current–voltage curves were measured at different temperatures by means of an Agilent 4284A LCR meter and a Keithley 617 electrometer.

Results and Discussion

The effective dielectric constant of the polycrystalline CeO_2 thin films was evaluated from the high-frequency ($f = 100$ kHz) *C-V* characteristics of the MOS devices and was found to be 25.5 in accumulation mode. Therefore, an equivalent oxide thickness of about 16.2 Å was estimated, taking into account quantum effects. At room temperature, the relevant *C-V* curve indicates the presence of the so-called "slow states," while at higher temperatures they show dispersion at depletion and inversion. The effect is well known from Si-based devices but is more significant when Ge is used as the substrate due to its smaller bandgap.[10] The D_{it} value at midgap calculated from the *C-V* curves at room temperature was around 1×10^{12} eV^{-1} cm^{-2}. As this value probably overestimates the true density of interface states,[10] it is also in agreement with the best results reported on similar devices with REOs as gate dielectrics.[2,4]

In order to understand the carrier transportation mechanisms of the CeO_2 dielectric, the temperature dependence of the gate-leakage current density (J_g) was investigated at the same temperature range (295–375 K) under both gate and substrate injection. As illustrated in Fig. 1, typical current densities at 295 K were about 0.4 mA/cm^2

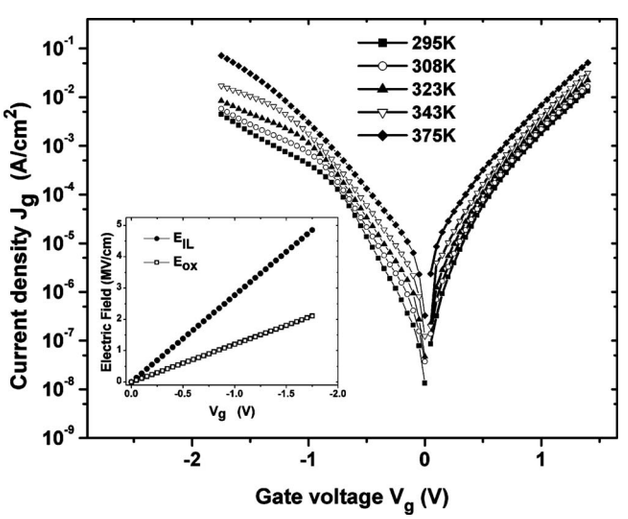

Figure 1. Current density J_g as a function of the voltage across the gate dielectric (7 nm CeO_2) of a Ge-MOS capacitor recorded from 295 to 375 K. Inset graph shows electric field in the Ce–O–Ge ILs and CeO_2 layers as a function of applied voltage as calculated from Eq. 1 and 2.

* Electrochemical Society Student Member.
z E-mail: eevagel@uoi.gr

at V_{FB}-1 V in accumulation and slightly higher at inversion. Also, the currents (at $V_{FB} \pm 1$ V) in both forward and reverse gate polarities are of the same order of magnitude, which indicates that the conduction mechanism is a bulk-limited[11] process. The rather high J_g values are consistent with the low energy gap of CeO_2 ($\sim$3.3 eV)[6] and the inevitably low band offsets.[4,6]

When CeO_2 is deposited on Ge, it reacts with the substrate, resulting in catalytic oxidation of Ge and spontaneous formation of a stable and thick Ce–germanate (Ce–O–Ge) interfacial layer (IL).[4] Assuming that no charge is accumulated at the CeO_2/germanate interface, the electric field across the two layers (IL and CeO_2) is given by[12]

$$E_{IL} = \frac{V_{applied}}{(\kappa_{IL}/\kappa_{ox})t_{ox} + t_{IL}} \quad [1]$$

$$E_{ox} = \frac{V_{applied}}{(\kappa_{ox}/\kappa_{IL})t_{IL} + t_{ox}} \quad [2]$$

where $V_{applied} = V_g - V_{FB}$ is the voltage applied to the gate dielectric stack and V_{FB} is the flatband voltage. The dielectric constant of the IL ($K_{IL} = 11$)[8] has been measured separately using a set of similarly grown MOS devices with different CeO_2 thicknesses (from 8 to 17 nm), while $\kappa_{ox} = 25.5$ was assumed for the CeO_2 layer; $t_{IL} = 1$ nm and $t_{ox} = 6$ nm are the relevant physical thicknesses as obtained from transmission electron microscopy[4] measurements. The electric field across each layer as calculated from Eq. 1 and 2 is shown in the inset of Fig. 1.

Two of the most frequently encountered current transport mechanisms for thin REO-films are the so-called Schottky and Poole–Frenkel emissions. After analyzing our data, space-charge limited currents as well as direct or Fowler–Nordheim tunneling currents have been excluded as the main leakage mechanisms due to the strong temperature dependence in the whole gate-voltage range. Schottky emission can be expressed as[13]

$$J_{SE} = A^*T^2 \exp\left[\frac{-q(\phi_b - \sqrt{qE_{ox}/4\pi\kappa_d\varepsilon_o})}{k_bT}\right] \quad [3]$$

where J_{SE} is the leakage current density, A^*(=143 A/cm^2 K^2) is the effective Richardson constant[14] for Ge (100), T is the absolute temperature, E_{ox} is the electric field across the oxide, q is the electronic charge, $\Phi_b(=q\phi_b)$ is the Schottky barrier height, ε_o is the free-space permittivity, κ_d is the dynamic dielectric constant (i.e., the electronic component of the dielectric constant), and k_b is the Boltzmann constant.

The Poole–Frenkel conduction mechanism is defined by the following field (E_{ox}) dependence of the current density $J_{P\text{-}F}$[13]

$$J_{P\text{-}F} = C_tE_{ox} \exp\left[\frac{-q(\varphi_t - \sqrt{qE_{ox}/\pi\kappa_d\varepsilon_o})}{k_bT}\right] \quad [4]$$

where C_t is a constant proportional to the density of bulk oxide traps, $\Phi_t(=q\varphi_t)$ is the depth of the trap's potential well, and other terms are as mentioned above.

For standard Schottky emission, a plot of $\log(J/T^2)$ vs $\sqrt{E_{ox}}$ should be linear. The dynamic dielectric constant is determined from the slope of the straight lines in these plots, and it should be equal to the optical dielectric constant κ_d, i.e., the square of the measured refractive index ($n^2 = \kappa_d$). In the case of gate injection, the data measured at all temperatures (295–375 K) and low to medium electric field ($\sim$0.1 to 0.9 MV/cm) fit the Schottky emission (Eq. 3) well, as shown in Fig. 2a. From the linear part of the curves, κ_d was found to lie between 3.4 and 3.9 with an error of $\pm$0.2. There is a systematic increase of κ_d with increasing T, but at the same time the experimental error in the obtained values of the slopes is rather high due to the uncertainty in the definition of the linear part of each curve. In the past, many groups have studied the dielectric properties of cerium oxides, and they reported κ_d values from around 2.0 up to 5.5. The lowest values were found on Au/CeO_2/Au metal-insulator-metal structures by Grosse et al.,[15] who also claimed that the κ_d values obtained when Poole-Frenkel emission dominated were significantly lower (1.6 vs 2.3) than in the case of Schottky emission. Al-Dahhan and Hogarth[16] have found $\kappa_d = 3.6$, but their structures were too complicated (Al–CeO_2/GeO_2–Al capacitors with thick oxide layers) and their results are under question. In a recent publication, Chiu reported κ_d values around 5.5 on Al/CeO_2/Si MOS devices[9] when Schottky emission dominates the current transport. The corresponding CeO_2 films were grown by rf magnetron sputtering and annealed at 400°C in N_2 ambient. In addition, the author found similar behavior with respect to the voltage ranges where Schottky emission dominates. The same results have also been shown in Hf–silicate-based devices,[17] although the conduction-band offsets are significantly higher. However, interesting information about the dielectric constant of CeO_2 films comes from an earlier work by Patsalas et al.[18] and Longothetidis et al.,[19] where the authors demonstrated a linear dependence of κ_d with respect to its mass density and deposition temperature. This result explains the above-mentioned wide spread of κ_d values and is in agreement with the observed wide range ($\kappa_d = 2.1$–3.8) reported on $NiSi/Gd_2O_3$/p-Si devices.[20] It could also explain the observed increase of κ_d with temperature.

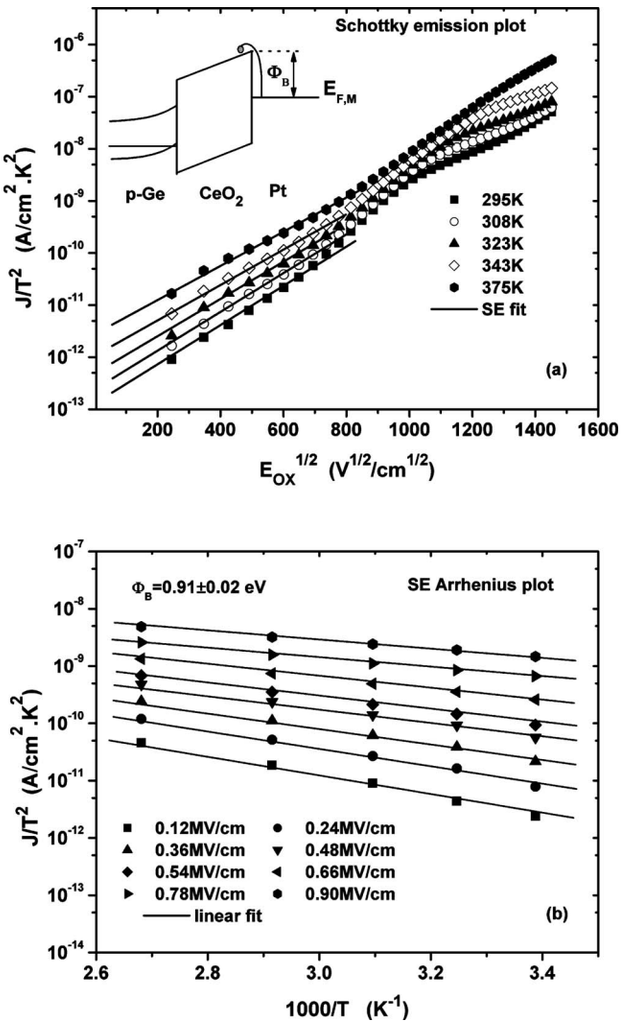

Figure 2. Schottky emission plots in the temperature range 295 to 375 K and low applied field under gate injection. The Pt/CeO_2/Ge band diagram is drawn as an inset.

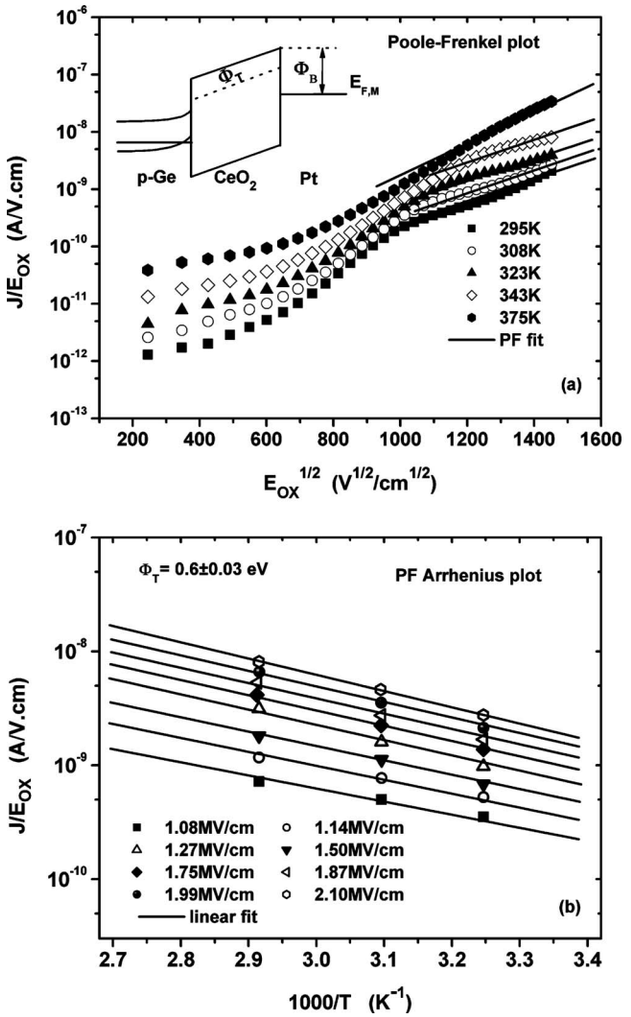

Figure 3. Poole–Frenkel conduction plots from 295 to 375 K under gate injection. The inset represents the band diagram while Φ_t is the energy level of the traps.

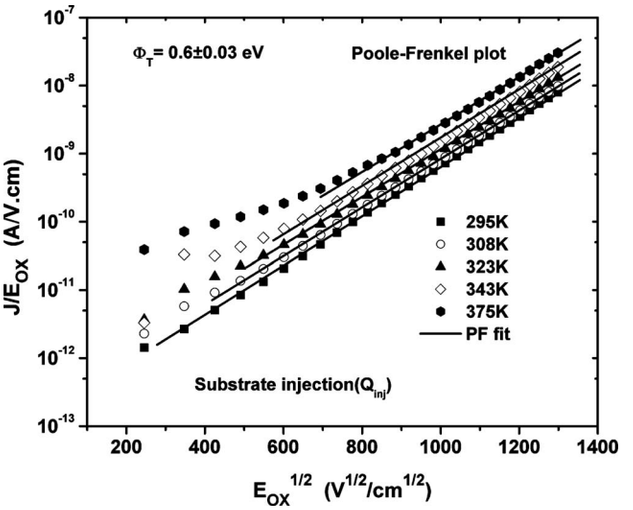

Figure 4. Poole–Frenkel plots for various temperatures at accumulation mode [substrate injection (Q_{inj})].

The Schottky barrier height at the Pt/CeO_2 interface was determined to be around 0.91 ± 0.2 eV using a plot of $\log(J/T^2)$ as a function of $1/T$, as shown in Fig. 2b. In the literature, the Schottky barrier height for Al/CeO_2 is about 0.7 eV[21] and 0.9 eV[15] for the Au/CeO_2 interface. It has also been reported that, at lower bias voltage range (≤ ± 1 V), the dominant current conduction mechanism in CeO_2 is Schottky emission.[7,9,15,21]

The Poole–Frenkel emission is presented in Fig. 3a, where $\log(J/E_{ox})$ is plotted as a function of $\sqrt{E_{ox}}$ for various temperatures. This semilog plot should be linear if Poole–Frenkel is the dominant conduction mechanism, and this is true for the higher E_{ox} values because of the band-bending and tunneling effects. This result is expected and has been reported for CeO_2 and other REOs in the past.[9,15,20,21] The dynamic dielectric constant was obtained from the slope of each Poole–Frenkel plot in Fig. 3a and was found to lie between 3.1 and 3.8 (±1), in good agreement with the values obtained from the analysis of the Schottky plots (Fig. 2a). However, the error in the determination of the κ_d values is slightly higher than in the Schottky case due to errors in the definition of the appropriate field range, where the curves are linear.

Moreover, the trap's energy level Φ_t was evaluated using Eq. 4 and the slopes of the Arrhenius plots in Fig. 3b. Various E_{ox} values have been used, and a mean activation energy of Φ_t = 0.60 ± 0.03 eV was obtained. This level has been plotted in the band diagram of the Pt/CeO_2/p-Ge structure shown as an inset in Fig. 3a and is highly probable to be related to oxygen vacancies or divacancies which have been theoretically predicted for a number of high-κ oxides.[22] The obtained Φ_t value is identical to those reported for Al/CeO_2/n-Si structures,[21] where the oxide films were E-beam evaporated and subsequently treated by rapid thermal annealing in N_2 ambient. A trap level of 1.12 eV was found in Al/CeO_2/Si MOS devices,[9] as well as a trap with a Φ_t value close to that in thin Gd_2O_3 films.[20] We believe that these results are in agreement with the theoretical work done on HfO_2 and La_2O_3 films,[22] where different charge states of the relaxed oxygen vacancy have been calculated in the forbidden gap of the oxides. Therefore, it is not surprising that different groups report on two defect levels in CeO_2.

Finally, the temperature dependence of the current transport mechanisms was studied in inversion mode (i.e., substrate injection). The Poole–Frenkel conduction mechanism was again dominant at higher gate voltages, which explains the similar behavior on both polarities of the J_g-V_g curves (Fig. 1). In addition, the obtained Φ_t value was exactly the same as for the accumulation mode as shown in Fig. 4. Furthermore, similar results have been obtained (not shown here for clarity) for other devices grown in the same way but with slightly different thicknesses of the CeO_2 films (8–10 nm).

Conclusions

In this article, the leakage current transport mechanisms of MBD-grown CeO_2 films on Ge substrates have been investigated. The electron (Schottky) barrier height at the Pt/CeO_2 interface was found to be equal to Φ_b = 0.91 eV, while a trap energy level with activation energy of Φ_t = 0.6 eV was detected in the oxide after analyzing the Schottky and Poole–Frenkel emission at lower or higher gate voltages, respectively.

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