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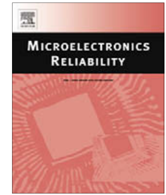

Study of stress-induced leakage current (SILC) in HfO_2/Dy_2O_3 high-κ gate stacks on germanium

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ABSTRACT

In the present work we study reliability issues of $Pt/HfO_2/Dy_2O_3$/n-Ge MOS structures under various stress conditions. The electrical characteristics of the micro-capacitors are very good probably due to the presence of a rare earth oxide as interfacial layer. It is shown that the injected charge (Q_{inj}) at high constant voltage stress (CVS) conditions induces stress-induced leakage current (SILC) that obeys a power-law. We also observe a correlation between the trapped oxide charge and SILC, which is, at low stress field, charge build-up and no SILC, while at high stress field SILC but few trapped charges. Results show that the present bilayer oxides combination can lead to Ge based MOS devices that show acceptable degradation of electrical properties of MOS structures and improved reliability characteristics.

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1. Introduction

Dielectrics of higher electric permittivity than SiO_2 (e.g. HfO_2, ~25) are investigated widely for their potential use as dielectric layers in advanced metal–oxide–semiconductor (MOS) devices [1,2] aiming to the substantial reduction of gate leakage currents [3]. An important consequence will be the use of thicker (higher permittivity) dielectric layers, and one would also expect to reduce the stress-induced leakage current and improve the reliability of the corresponding devices [4]. During the past decade, germanium (Ge) based MOS devices are extensively studied due to its high mobility [1,2] for the future semiconductor and integrated circuits industry. Nevertheless, not much experimental work has been devoted on the oxide degradation and reliability of high-κ dielectrics for the corresponding MOS devices. Rare earth oxides (REOs) are friendly with Ge substrate, so they can be used as an interfacial buffer layer, REOs can also be deposited directly on Ge [5]. The reason is that REOs react strongly with the substrate resulting in catalytic oxidation of Ge and in the spontaneous formation of stable interfacial layers, such as germanate (e.g. La–O–Ge [6], Ce–O–Ge [7]). This germanate layer could be responsible for the reduction of hysteresis and interface state density (D_{it}). Alternative gate dielectric stacks usually consist of an ultrathin interfacial buffer layer (e.g. Dy_2O_3) and a metal oxide layer with higher electric permittivity (e.g. HfO_2) and a typical thickness of 3–10 nm. The gate stack that we are studying is HfO_2/Dy_2O_3 grown on n-type Ge with Pt gate electrode. In the present work we have noticed a formation of germanate compound (Dy–Ge–O) at the interface of Ge/Dy_2O_3, which is not shown here.

The first observation of leakage current in thin dielectric layers subjected to high electrical stress field date back to the work of Maserjian and Zamani [8]. This current is commonly termed as stress-induced leakage current (SILC) [9]. SILC is one of the main limits in the scaling down of deep-submicron technologies; in fact SILC appears long before the occurrence of hard and/or soft breakdown, further reducing the lifetime of devices. Moreover, this SILC hampers the long-term reliability of non-volatile memories, leading to charge loss from the floating gate [10–12] while it can affect dynamic logic and related components. Many papers have been published studying SILC and its relation to device lifetime [8–10]. Quite often accelerated life tests of MOS capacitors are performed by applying a high constant voltage at the gate contact (constant voltage stress, CVS) or by injecting a constant current across the oxide (constant current stress, CCS) over a period of time. The degradation of the oxide is generally monitored by periodically interrupting the stress to allow for electrical measurements, e.g. SILC, flatband voltage shift (V_{fb}), charge trapping, etc. Stress-induced leakage current ($J_{SILC} = J_g - J_0$) is defined as the increase in oxide leakage current density after a high field stress (J_g), as compared to the leakage prior to any stressing (J_0) [13]. Generation of SILC is also modeled by different studies [8,12–15].

In the present work, we report on the increase in the gate SILC during constant voltage stress [12,16] of HfO_2/Dy_2O_3 gate stack dielectrics. REOs such as Gd_2O_3, CeO_2, Dy_2O_3, La_2O_3 have been leading candidates in the quest to replace the traditional SiO_2 gate dielectric of MOS transistors with a material having higher dielectric constant (κ = 12–23) [6,7,17–19]. REOs can be directly deposited on Ge showing better electrical characteristics than Si with

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low interface density ($D_{it} \sim 10^{12}$ eV/cm^2 or below) [17–19]. Unfortunately, till now all of the REOs seem to share two deficiencies. First, they cause a SiO_2-like interfacial layer to grow when they are deposited on Silicon (Si) [20]. Second, they also produce electrical instabilities in MOS devices. Electrical instabilities have been the subject of numerous experimental studies [21–27], and it seems possible to interpret many of these as arising from the trapping of charge somewhere with in the gate stack. The SILC variation that we have observed in our study, can not be simply interpreted as a displacement current deriving from charging/discharging of oxide defects close to the interfaces [8]. Charge trapping at the interface between the two dielectric layers of a high-κ gate stack is also studied as the two layers have different compositions which means they will have also different conductivities (and transport mechanisms). When the gate bias is applied, the application of a gate bias will immediately produce a discontinuity in current density at the interface between the two layers, causing charge accumulation there until, in steady-state, the same current density flows through the both layers. If the gate bias is removed, a discontinuity in current density will again be produced, this time causing the charge to rush out of the gate stack [28,29].

2. Experiment

Dy_2O_3/HfO_2 oxide stacks were prepared by atomic oxygen beam deposition on *n*-type Ge(100) with resistivity ~0.02 Ω-cm. Native oxide was desorbed in situ under UHV conditions by heating the substrate to 360 °C for 15 min, until a (2 × 1) reconstruction appears in the (RHEED) pattern, indicating a clean (100) surface. Subsequently, the substrate was cooled down to 225 °C where the oxide stacks were deposited. The surface was exposed to atomic oxygen beams generated by an RF plasma source with the simultaneous e-beam evaporation of Dy/Hf at a rate of about ~0.15 Å/s. The total nominal thickness of the film was approximately 11 nm (10 nm HfO_2/1 nmDy_2O_3). MIS capacitors were prepared by shadow mask and e-beam evaporation of 30-nm-thick Pt electrodes to define circular dots, 300 μm in diameter. The back ohmic contact was made using eutectic InGa alloy.

The devices have been subjected to electrical stress under CVS conditions with the Keithley 617 meter. We took successive stresses of 1000 s at two different fields (3 MV/cm, 4 MV/cm). After each stress cycle the gate bias was interrupted for a while in order to measure current density–gate voltage (J_g–V_g) and current density–stress time (J_g–t) curves, with the simultaneous acquisition of a high frequency (hf) capacitance–voltage (C–V) curve for the determination of the flatband voltage shift (ΔV_{fb}) by using a pulsing technique (also known as 'stress and sense'), more details are described elsewhere [30]. The C–V measurement was obtained using an Agilent 4284A LCR meter. Fresh devices were used for each stress measurement.

3. Results and discussion

The current density (J_g) as function of time (t) is shown in Fig. 1a at CVS condition, where constant stress field is 4 MV/cm and the solid line is used as a guide line to the eye. The experimental result shows initially the current density (J_g) decrease until to a turn around point, after that it follows an increase of J_g, finally reaches a saturation value of J_g with respect to stress time (t). The possible explanations of Fig. 1a are following: (i): we observed in the first few seconds a decrease of current and then an increase of stress current, the current passes through a minimum, which could seem to indicate the creation of positive charges as well as filling at the pre-existing fixed oxide traps, responsible to the decrease of current. After a few seconds of stress it reaches to a turn around point,

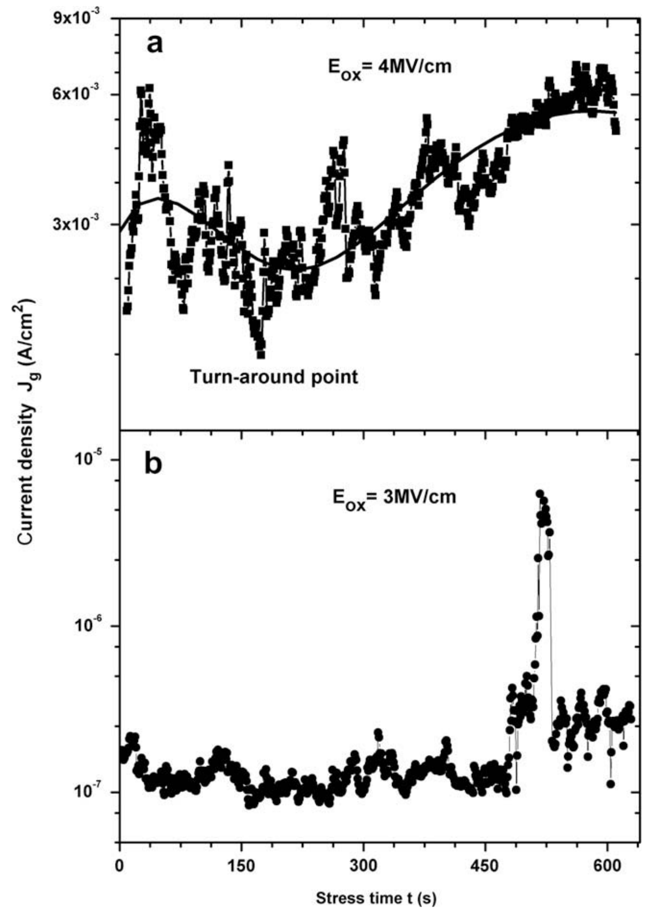

Fig. 1. The Fig. 1a shows current density (J_g) versus stress time (t) graph at high field. Initial current decrease and final transient increase are observed. The solid line is guide line to the eye. While a J_g as a function t at low stress field displays in Fig 1b.

and then the creation of negative charges (bulk/interface) responsible for the J_g increase. Eventually after long time stress it reached to breakdown (BD). To see the BD mechanism quite a long time is needed, the result is not shown here. We conclude that the creation of new defects are gradually increasing and then slows, finally the upward exponential curve reaches saturation. (ii) This could also be explained with two simultaneous mechanisms together, namely, Maxwell–Wagner instability [29] and relaxation effect of the bilayers [31]. This metal–oxide high-κ behaviour is contributed by dielectric polarization/relaxation and charge trapping/detrapping together. In the experimental data, the J_g noise level could be explained with the above mechanism Maxwell–Wagner instability [29] that we have detailed before. While at low stress field (3 MV/cm) we notice the slight decay of current with respect to stress time (Fig. 1b). The change of the J_g is almost negligible, could be a random trapping/detrapping mechanism and after 479 s we notice a sudden increase of J_g may a soft breakdown (SBD), finally J_g remains the same leakage level. After a quite long time J_g starts increasing, the result is not show here. Interesting thing is that we have noticed in the measurement is sometime the J_g increases and sometime decreases keeping the current leakage level almost of the same order could be referred as noise; basically the J_g trend is decreasing with respect to stress until a long stress time, which is not fully understood. This could be explained as contributions of both relaxation and Maxwell–Wagner instability together [32]. The charges are accumulated at the interface of the gate stack; suddenly find a percolation path causes increase of J_g and/or detrapping path decreases J_g.

Stress-induced leakage current (SILC) through the gate dielectric of a MOS capacitor causes an additional power consumption which, although tolerable in currently used technologies, is unwanted especially in low-power applications; there it may become a reliability issue in those deep-submicron technologies where SILC dominates over tunneling current. We have introduced previously CVS and SILC. The CVS method [1,15] was used to study the SILC at various stress fields (E_{ox}) with respect to time. Two different stress fields (3 MV/cm and 4 MV/cm) were applied on the same area of 7×10^{-4} cm^2 of different capacitors successively, immediately after each stress the leakage current density (J_g) as a function of gate voltage (V_g) i.e. J_g–V_g curves were also measured. Fresh capacitors were used for these measurements during each different stress field.

Gate current density (J_g) as function of applied gate voltage (V_g) are shown in Fig. 2, where J_g–V_g curves were taken after each stress of 1000 s at 4 MV/cm. The increase of current density is distinctly exemplified after each stress and from the curves we notice SILC. It is the increase in low level leakage across a thin gate oxide after the oxide has been subjected to a high electrical-field stress. SILC (J_{increase}) can be given by J_g–J_o, where J_o and J_g are the gate current densities at a given bias before and after stressing the device, respectively. However the different behaviour was observed at low stress field (3 MV/cm) case which is illustrated in Fig. 3 where shows J_g–V_g curves of fresh and after successive stresses on the same device. Here we have observed that the current decreases slightly as function of stress time (i.e. charge injection), resulting in negligible and insignificant SILC. So, that infers SILC is field dependent, i.e. at high stress field creation of new defects is evident [9] and on the other hand, at low field it explains anomalously [33]. This means that there is no SILC at low stressing which perhaps is opposite from higher stress; and that SILC contributes mostly in gate leakage current. Also it is worth mentioning that the leakage current density at $1\,\mathrm{V} \pm V_{fb}$ is found to be around $\sim 10^{-8}$ A/cm^2, which is very low level leakage current indicating a good integrity of the gate stack.

When the applied CVS field is low (Fig. 3), we have observed that SILC is slightly decreasing, virtually is negligible. Two mechanisms can be claimed as responsible for SILC decay [29]: (a) "clogging" of oxide neutral defects and (b) trapping of negative charge in the bilayer interfaces. Based on the first mechanism, electron trapping could likely occur just on the weak spots, which arbitrate SILC. Later, a local relaxation of oxide lattice may lead to the annealing of the defect, resulting in the either weak or strong bond. It is also possible that relaxation could result in such a deep trap, that electrons are no longer available for SILC conduction. Alternatively, electrons could be trapped also by deep defects other than those directly involved in the current transport. The SILC generation kinetics follows a universal power-law [34].

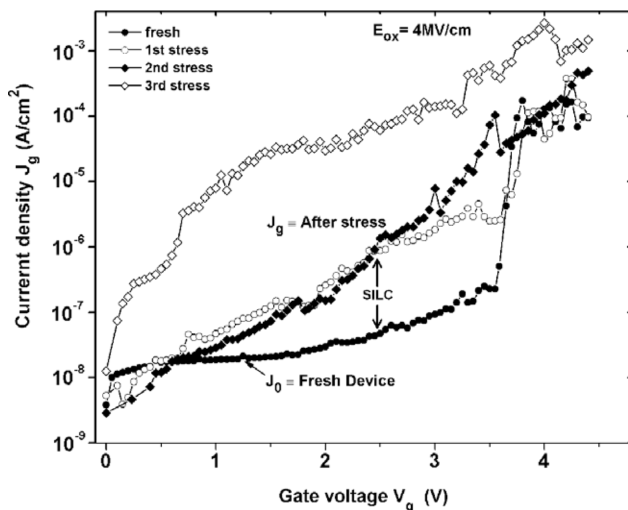

Fig. 2. The figure shows the gate current density J_g versus bias V_g before and after high successive stress.

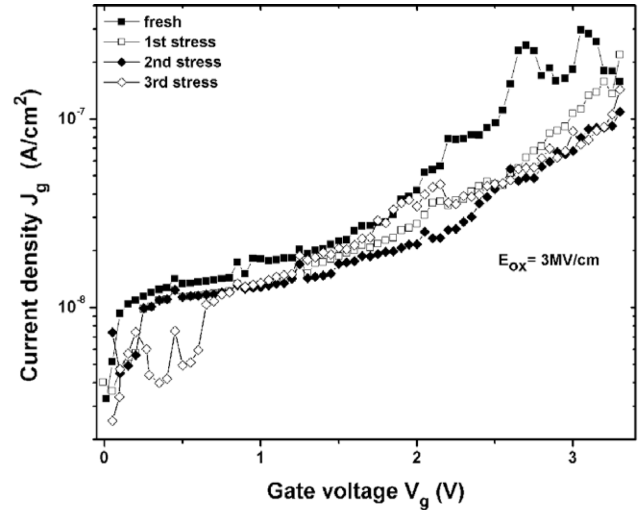

Fig. 3. Typical J_g–V_g curves plotted before and after a low stress field and it reveals negligible SILC values.

$$\delta \ln(J_{\mathrm{SILC}})/\delta Q_{inj} = K_e N_{inj}^{v}, \tag{1}$$

where, K_e is a parameter that depends on oxide thickness and oxidation technology, $N_{inj} = Q_{inj}/q$; N_{inj} is the number of injected charge, Q_{inj} is the total charge injected, $q = 1.6 \times 10^{-19}$ C is the elementary charge, where the injected charge (Q_{inj}) is calculated from the fundamental equation:

$$Q_{inj} = \int_0^t J_g(t)dt, \tag{2}$$

here, J_g is current density. The kinetics law applies to all constant voltage stressed devices, regardless of their oxide thickness or oxidation process. Integrating Eq. (1) we find

$$J_{\mathrm{SILC}} = J_{sat} \exp(-D/Q_{inj}^{\alpha}), \tag{3}$$

in which, $\alpha = -(v-1)$, $D = K_e/\alpha$, while J_{sat} is an integration constant. The power-law describes well the experimental behaviour of SILC, predicting saturation at a value J_{sat} for high injected charges. The parameter K_e appearing in Eq. (1), and also in D in Eq. (3), is related to the growth rate of SILC. Fig. 4 shows the stress-induced leakage current (J_{SILC}) versus injected charge (Q_{inj}) during the stress. We use Eq. (3) to fit our experimental data (Fig. 4). The value of v is found to be -1.37 for oxide thickness t_{ox} = 11 nm while the value of v has been reported from -1.1 to -1.4 [16,34].

Stress-induced leakage current is used to monitor the oxide degradation and to predict the oxide's behaviour under low voltage stress. Oxide degradation is usually quantified by the normalized excess SILC ($\Delta J/J_o$) due to stress; also it is related to the injected charges across the gate dielectrics. The normalized current density increase is defined as $\Delta J/J_o$, where $\Delta J = J_g$–J_o. One observes for different stress voltages that $\Delta J/J_o$ changes (increases or decreases) with respect to the injected charges and follows a power-law [35]

$$\Delta J/J_O = BQ_{inj}^{\gamma}, \tag{4}$$

where, B and γ are SILC-related parameters obtained from our experimental data. B is the leakage current cussed by the traps generated during stress and γ corresponds to the trap generation rate.

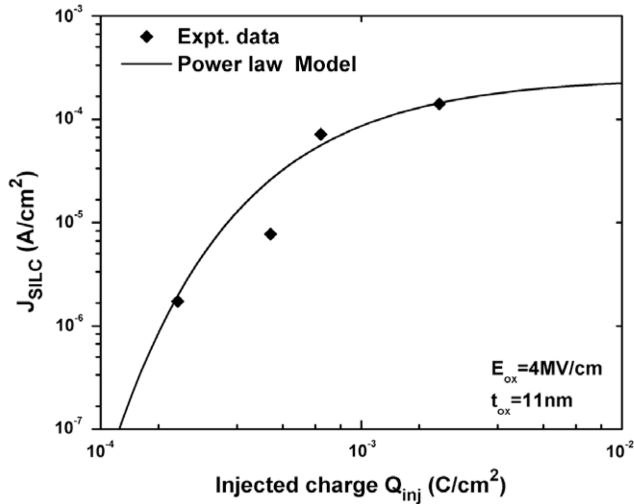

Fig. 4. Experimental data of SILC (symbol) and corresponding simulation (solid line) obtain from Power-Law Model (Eq. (3)) after CVS at 4 MV/cm.

The normalized excess gate leakage current ($\Delta J/J_o$) is plotted as a function of injected charge (Q_{inj}) at two different gate stress voltages. Each CVS was performed at room temperature. Initially, at high field, in log–log plot, SILC increases linearly. Following a large electrons injection (long stress time), usually SILC reaches to saturation. In the figure, at high field (4 MV/cm), SILC doesn't reach perfect saturation; the injected charge is perhaps too low. But, it interesting to note in Fig. 5, at low stress field, we do not observe SILC variations, i.e. equal to 0, so we may conclude SILC is almost negligible. Eventually, at low field, DiMaria and Carlier [14] did not observe saturation of SILC not even a decrease. It was also reported initially the SILC was increasing linearly with electron fluence; at large fluence the saturation of SILC was observed. In our study, as the positive high gate voltage is applied, a large number of traps (or broken bonds) are generated within the gate dielectric layer and in the interface [36]. We assume that these traps are randomly occupied within the oxide. When a critical number of traps are generated, they will form a percolation path between the gate and the substrate, leading to a sudden increase in gate current which may cause oxide breakdown [37]. In addition, the electrons injected from n-Ge substrate get trapped in the pre-existing traps in the oxides. Under the long stress time, the number of unoccupied trap states available for electron trapping will decrease and the decreased number of available traps will reduce the net trapping rate so that the SILC becomes saturated after the initial stress time [33]. Fitting Eq. (4) to the experimental data we have found the value of γ for 3 MV/cm and 4 MV/cm to be -0.1 and 0.89, respectively. So, at low field the negative value indicates the creation of a few interface traps and the pre-existing traps at the interface of the gate stacks are filling-up; as a result, there are not enough defects/traps available. On the contrary, at high field it indicates a high rate of creation of new traps in the bulk of the oxide.

Maserjian and Zamani reported that charge assisted tunneling by the charge build-up in the oxides resulted in excess current during stressing [8]. The oxide trap charge build-up (Q_{ot}) can be measured from the flatband voltage shift, using hf C–V technique. It has also been reported that flatband voltage shift (ΔV_{fb}) is a tool to calculate the trapped charge ($Q_{ot} = \Delta V_{fb} C_{ox}$ [38], where C_{ox} is oxide capacitance) in the bulk of the oxide during CVS [39]. In analogy to Eq. (4), the flatband voltage shift and injected electron fluence can be expressed as empirical power-law according to Kumar et al. [39] as:

$$\Delta V_{fb} = \Delta V_{\max} Q_{inj}^{\delta}, \quad (5)$$

here, $\Delta V_{\max}$ is a constant, which is defined as the maximum flatband shift during each stress and δ is the exponential power. Fig. 6 displays the flatband voltage shift (ΔV_{fb}) as a function of injected electron fluence (Q_{inj}) at two different fields, which investigates the oxide charge build-up [15]. At low field (3 MV/cm) ΔV_{fb} is higher than that of high field (4 MV/cm). So at low field more negative charges are trapped although at higher field the charge trapping is less. During low stress field the charge build-up is dominant process to the creation of new traps/defects, while at higher field the charge trapping mechanism is rather faint. Fitting Eq. (5) to the experimental data, we found the δ values to be 0.15 and 0.41 for 3 MV/cm and 4 MV/cm, respectively. The compatible results (δ = 0.1–0.9) have been reported from other researchers [40–42]. In a recent work [30], it was reported that at higher stress field the amount of trapped charge is more than that of at low stress field, which is different from our present work. It is not quite under-

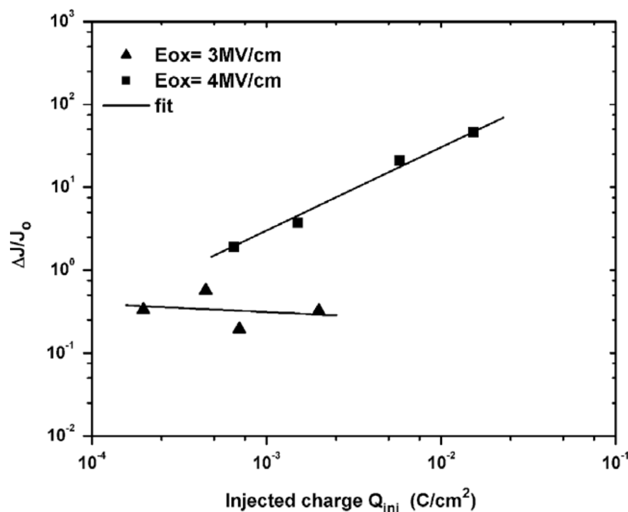

Fig. 5. Normalized leakage current ($\Delta J/J_0$) versus injected charge Q_{inj}, measured at two different electric fields (4 MV/cm & 3 MV/cm) after successive stress of 1000s with CVS methods. Symbols indicate the experimental data and solid lines the fit by Eq. (4).

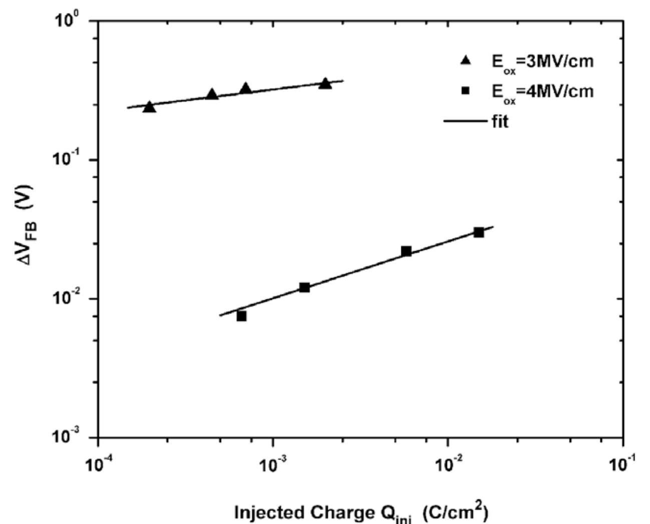

Fig. 6. Flatband voltage shifts ΔV_{fb} versus injected charge fluence Q_{inj} at two CVS electric fields (3 MV/cm & 4 MV/cm). Symbols indicate the experimental data and solid lines the fit by Eq. (5).

standable, could be that the present dielectric is gate stack (HfO_2/Dy_2O_3) while other was single layer (CeO_2). It is also noticeable that the amount of trapped charges of the present gate stack is lower than that of CeO_2 single layer. As we mention before, due to different-κ dielectric layers there was present the Maxwell–Wagner instability and in the same time because of the gate stack of high-κ HfO_2 ($\kappa \sim 25$) with Dy_2O_3 ($\kappa \sim 12$–14) the relaxation effect was present. We have noticed that at low stress field the relaxation is more effective mechanism in this gate stack [32]. However, in this structure of gate dielectrics there were basically three layer e.g. germanate (Dy–Ge–O), Dy_2O_3 and HfO_2 (result is not shown here), so finally there were three interface where the charge trapping was dominant mechanism. Similar relaxation effect was also observed in other gate stacks e.g. HfO_2/SiO_2 [22,29], $ZrHfO/SiO_2$ [31].

4. Conclusion

In the present work we have investigated reliability issues of the gate stack of HfO_2/Dy_2O_3 namely stress-induced leakage current, flatband voltage shift and charge trapping in the interface of bilayers. It was the first time, to our knowledge that this gate stack on Ge substrate was studied. The value of leakage current density at $1\,V \pm V_{fb}$ was extremely low ($\sim 10^{-8}$ A/cm^2), which indicates good dielectric property of the gate stack. Studying SILC we found that at high field it increases and obeys a power-law; on the contrary, at low field it was not visible. Moreover, at high field, initially (under CVS) there was more charge trapping at the pre-existing traps at the bulk/interface followed by the creation of interface defects and later was the creation of a large number of neutral defects which cause SILC. This elucidates the correlation of charge build-up and SILC. We have found from our study that at low stress charge trapping is a dominant process over SILC, while at high stress field situation reverses i.e. charge trapping is faint but SILC is prevailing. The characteristic SILC phenomenon is observed regardless of substrates (either Si or Ge) and has a similar behaviour. The power-law models of SILC proposed for Si-substrate could be used for Ge substrate. From the experimental evidence, low SILC betokens for the future high performance, reliable gate stacks for CMOS Technology.

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