Correlation of Charge Buildup and Stress-Induced Leakage Current in Cerium Oxide Films Grown on Ge (100) Substrates

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***Abstract*—High-κ films are currently deposited on Ge substrates to compensate the mobility loss, as Ge offers higher mobility compared with that of silicon. This paper deals with the reliability characteristics of cerium oxide films grown by molecular beam deposition on n-type Ge (100) substrates. MOS capacitors with Pt gate electrodes were subjected to constant voltage stress conditions at accumulation. The correlation of the charge-trapping characteristics and the stress-induced leakage current (SILC) to the applied field is observed and analyzed. The results suggest that one major problem for the potential use of rare earth oxides in future MOS technology is the existence of relaxation effects. The cross-sectional value of the bulk oxide traps is on the order of 10^{-18} cm^2, thus indicating neutral defects. Direct comparison to reported results on high-κ/Si and SiO_2/Si structures shows that SILC properties are related to the quality of the dielectric layers; the semiconductor substrate is immaterial.**

***Index Terms*—Cerium oxide (CeO_2), charge trapping, Germanium (Ge), rare earth oxide (REO), stress-induced leakage current (SILC).**

I. Introduction

As TRADITIONAL scaling becomes increasingly difficult, germanium (Ge) and other high-mobility semiconductor channels may offer performance enhancement in MOSFETs beyond that obtained with Si-based devices [1]–[4]. The introduction of high-κ dielectrics as potential replacements for SiO_2 has also benefited Ge MOS devices, and relevant research has been revived recently [5]. The basic requirements of a replacement gate dielectric are, among others, suitably high permittivity, appropriate band gap, band alignment to Ge, chemical stability with the substrate materials (Ge), and process compatibility. There are a number of other requirements for a new gate dielectric material, such as process compatibility and reliability. A systematic consideration of the required properties of gate dielectrics reveals a number of important properties for selecting an alternative gate dielectric. Unfortunately, the unstable native oxide of Ge was one of the biggest obstructions in very large scale integration of CMOS devices in Ge. Rigorous interface engineering and characterization are therefore necessary to obtain excellent electrical performance of Ge transistors with high-κ gate dielectrics. So far, it has been reported that one possible solution is the deposition of a thin GeO_xN_y film on the Ge substrates prior to HfO_2 deposition. The corresponding p-MOSFETs showed a twofold enhancement in mobility; however, the interface state density remained very high [2].

Despite this progress, a number of issues remain unresolved, such as the unexpected threshold voltage ($V_{\rm th}$) positive shift in p-MOSFETs [6]–[8] or the poor performance of n-MOSFETs. There is a need for better understanding of the interfacial properties on one hand and for alternative passivating layers or high-κ dielectrics on the other [9]. An alternative approach to the passivation problem could be the use of rare earth oxides (REOs) [10]. A number of these oxides, such as La_2O_3, CeO_2, Gd_2O_3, and Dy_2O_3, can be deposited directly on Ge with improved electrical characteristics [11]–[13]. One of the important reliability issues for the potential use of REOs in future Ge-based MOS devices is the study of the effects from the application of electrical stress on the density of the preexisting and on the creation of new oxide defects. The case of ceria has been studied extensively [14], [15], showing that CeO_2 reduces the density of interface states to 10^{12} cm$^{-2}\cdot$ V^{-1} or below [5]. This is a substantial improvement with respect to molecular beam deposition (MBD)-prepared HfO_2/GeON structures. On the other hand, CeO_2 suffers from leakage current since it has a low band gap of about 3.3 eV [16]. In addition, an interfacial layer is spontaneously formed, increasing with film thickness and deposition temperature [13], which makes gate scaling difficult. Using CeO_2 as an ultrathin passivating layer and combining it with a HfO_2 cap, leakage is improved, resulting in long-channel functional p- and n-MOSFETs [17]. In terms of transistor behavior, this, as a consequence, reduces the $I_{\rm OFF}$ current producing p-MOSFETs with exceptionally high $I_{\rm ON}/_{\rm OFF}$ ratio $\sim 10^6$ [17], which is one of the best values reported in the literature. This property is regarded as indirect evidence that CeO_2 acts as a good passivating layer of interface defect states; however, the $I_{\rm ON}$ current and the channel mobility remain low [17], which points to the need for a better passivating material.

Among the various problems arising when a high-κ material is to be used in future MOS devices, relaxation and charge-trapping effects need special attention.

Charge trapping is a common phenomenon observed in most high-κ dielectric materials [18]. During device operation, some charge may be trapped as it passes through the gate stack, causing device instabilities such as threshold voltage ($V_{\rm th}$) shifts and drive current degradation [19], [20]. Compared

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with SiO_2, charge trapping in high-κ is much more severe [18]–[23]. The mechanism of charge trapping is generally believed to be mostly due to trapping on preexisting defects in the high-κ layer and/or its interfaces. New traps can also be created under certain conditions (e.g., under high gate bias stress or hot-carrier injection [24]). There seems to be a correlation between charge trapping and reduced channel mobility, which is another important issue for high-κ devices [19], [20]. Films with improved charge-trapping characteristics appear to have better electron mobility. Excessive charge trapping also invalidates measurements of channel mobility because neither charge in the semiconductor inversion layer nor effective electric field within the dielectric can be calculated accurately.

It has already been proved in Si-based MOS devices that there is a strict correlation between the neutral electron traps and the mechanism of injected electrons at low voltage, which gives rise to stress-induced leakage current (SILC) [25], [26]. However, neutral traps cannot be measured directly because of their electrical neutrality. Therefore, SILC generated during constant voltage stress (CVS) has proved to be a very sensitive degradation monitor at low voltages [27], [28], while accurate SILC measurements require a well-controlled experimental environment, and temperature stability is a very critical issue.

On the other hand, relaxation in a solid involves the recovery of strain when the stress changes [29]. Dielectric relaxation is a bulk-related phenomenon, which causes relaxation current following the direction of dV/dt. It has been detected in polycrystalline, disordered, or amorphous films but not in single-crystal dielectrics [30]. When an external field is applied across a film, it separates the bound charges. This results in polarization and a compensating internal field. When the external field is released, the internal bound charges are neutralized by the hopping of free charges, while a remnant polarization and an internal field still remain in the film [29]. As the dielectric film has very low conductivity, this is a slow process, in which the relaxation current decays with time following the Curie–von Schweidler law [30] $J/P = a/t^{-n}$, where J is the relaxation current density (in ampere per square centimeter), P is the total polarization or surface charge density (in volts nanofarad per square centimeter), t is time (in seconds), a is a constant, and n is a real number close to one.

As reported in [29], the relaxation currents measured in high-κ films were one to two orders of magnitude larger than that of SiO_2. The result is consistent with the atomic configuration of high-κ dielectrics. Considering that the metal–oxygen bonds lack symmetry, the centers of the positive and negative charges do not coincide after an applied electric field has been removed. Hence, dipoles are easily created in high-κ dielectrics. Considering the larger magnitude, relaxation currents are easily observed on high-κ films, while it further impacts the film's behavior. This is because the existence of relaxation current indicates that the bulk film still maintains its integrity after the stress; however, on the other hand, this transient current can shift flatband voltage, hence severely deteriorating the performance of a MOSFET by shifting the threshold voltage and delaying the switching time [31].

The study of charge trapping/detrapping and relaxation phenomena has been mostly probed on silicon (Si). In particular, charge trapping is being actively investigated for silicon on various high-κ gate dielectrics, such as silicon nitride (Si_3N_4) or oxynitride (SiON) [32], titanium oxide (TiO_2) [33], zirconium oxide (ZrO_2), [34], [35], hafnium oxide (HfO_2) [18], [36], [37], and aluminum oxide (Al_2O_3) [38].

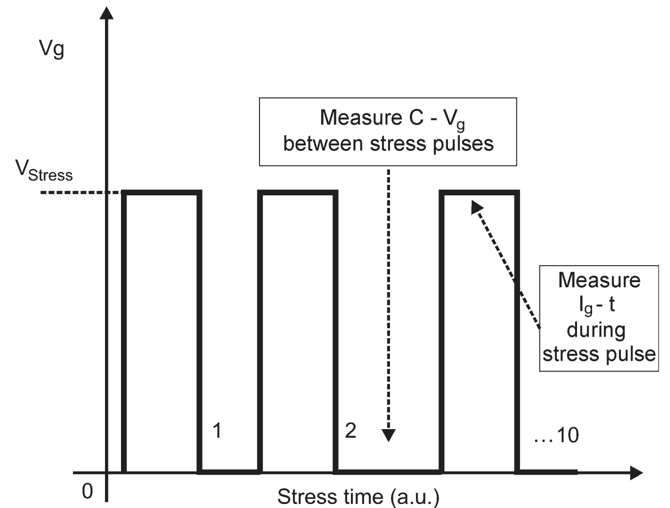

Fig. 1. Illustration of the "stress and sense" technique used for charge buildup and SILC measurements.

Relevant work on germanium (Ge) substrate is rather inadequate and is the main subject of this paper. In particular, $Pt/CeO_2/n$-Ge MOS capacitors are subjected to CVS conditions at accumulation, and the observed trapping/relaxation phenomena are presented and analyzed. It will be demonstrated that oxide degradation occurs under high stress field conditions ($E_{ox} \sim 3$ MV/cm) and that extrapolation of the obtained results to normal operating conditions are indeed possible, provided that the correct model is used. However, at the lower field regime, it will be shown that relaxation effects are responsible for the observed "anomalous" results.

II. Experimental

Cerium oxides and thin insulating films were grown on n-type Ge (100) substrates using MBD. The layers were deposited directly on n-type Ge by atomic oxygen plasma beam from an e-beam evaporator. MIS capacitor structures were fabricated using a shadow mask so that the top gate contacts were deposited by Pt and the bottom ohmic contact was made by eutectic In–Ga alloy. The samples were subsequently annealed at forming gas environment at 200 °C for 20 min. The thickness (t_{ox}) of the samples was estimated by X-ray reflectivity measurements to be 10 nm approximately. The area of the capacitors was 7×10^{-4} cm^2. The capacitance voltage (C–V_g) and current versus time (J_g–t) characteristics of the MOS capacitors were studied using an Agilent 4284A LCR meter, a Keithley 617 electrometer, and appropriate programming. Charge-trapping properties were studied by implementing a pulsing technique (also known as "stress and sense") shown in Fig. 1. More details are given elsewhere [39]. The SILC measurement was assessed by applying a CVS at accumulation for a finite period of time (1000 s) while monitoring the leakage current repeatedly (J_g–t curve). All the measurements were done in a dark box and at room temperature. The maximum

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change of temperature during the experiment never exceeded ± 0.2 °C. Fresh devices were used for each stress measurements. The applied field $(E_{\rm ox})$ across the dielectric $(\mathrm{CeO_2})$ was calculated by $E_{\rm ox} = (V_{\rm ox}/t_{\rm ox})$, where $V_{\rm ox} = V_g - V_{\rm FB}$ is the voltage applied to the gate dielectric stack, V_g is the gate bias voltage, and $V_{\rm FB}$ is the flatband voltage assuming that no charge is accumulated at the Ge/$\mathrm{CeO_2}$ interface.

III. Results and Discussion

An overview of this section is as follows. First, we show that an analysis of the high-frequency (hf) C–V_g hysteresis loops gives a rather clear indication for the evolution of both interface and bulk oxide defects. Second, we examine the gate current, whose increase with time during moderate field stressing suggests the buildup of negative charge together with the creation of new defects in the dielectric. Third, we study the evolution of the gate current after the application of a low forward CVS bias where relaxation effects are present. Fourth, we investigate the change of both the buildup charges and SILC coefficients with the applied forward stress, in order to estimate whether the reliability results obtained after CVS at higher fields can be extrapolated at typical MOS operating fields. Finally, we calculate and discuss the capture cross section of investigated traps.

A. Change of "Border Traps" With Stress

In a pioneering paper, Fleetwood *et al.* [23] introduced the concept of "border traps" as a new subclass of defects commonly appearing in MOS devices. These defects lie physically within the oxide but are near enough to the semiconductor/oxide interface, and they often act indistinguishably from interface traps. In electrical measurements at a given effective frequency, interface and border traps close enough to the interface and/or at appropriate energies can change charge states (for example, during a C–V_g or I_g–V_g ramp) if they can communicate with the semiconductor (Ge, in this case) on time scales faster than the characteristic measurement times. Bulk oxide traps which do not communicate with the Ge on the measurement time scale are considered here as bulk oxide states following the common nomenclature of electrical characterization of MOS devices.

One measure of the effective border trap densities can be obtained from C–V_g hysteresis [23]. It is rather obvious that the slower the ramp rate, the more border traps can exchange charge with the Ge substrates. Here, a ramp rate of $\sim$0.1 V/s was used, corresponding to switching times of $\sim$40 s over the portion of the curve showing hysteresis. Border traps with switching times slower than this will be counted as bulk trapped charges in these measurements, and those with switching times comparable to that of interface traps ($\sim$1 ms or less) will be counted as interface traps.

However, a better measure of the effective border trap density $\Delta N_{\rm bt}$ can be obtained by integrating the absolute value of the difference between the hf C–V_g curves, i.e.,

$$\Delta N_{\rm bt} \approx \frac{1}{qA}\int |C_r - C_f| dV. \quad (1)$$

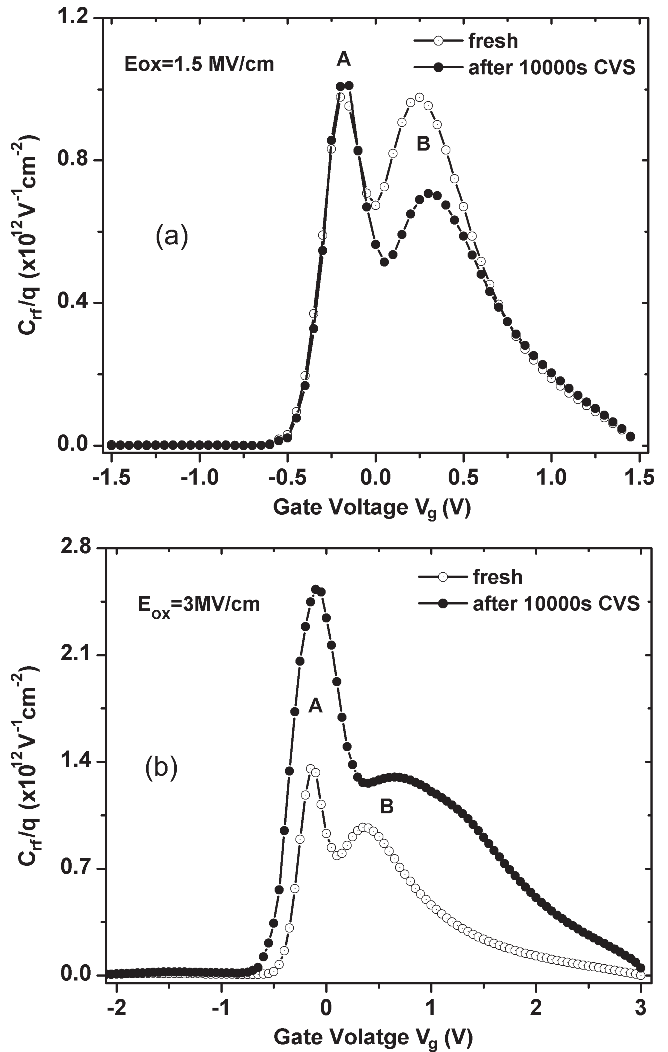

Fig. 2. Border-trap density per unit energy $(C_{\rm rf}/q)$ versus gate voltage V_g for the case of (a) low applied field across the oxide ($E_{\rm ox} = 1.5$ MV/cm) and (b) high field ($E_{\rm ox} = 3.0$ MV/cm). Peak A is mainly due to the interface defects while peak B is attributed to bulk oxide defects only.

The C–V_g difference curve $C_{\rm rf}(V_g) = (C_r - C_f)$ is a function of the applied gate voltage. The indexes refer to measurement from accumulation to inversion ($C_r = C_{\rm reverse}$) and inversion to accumulation ($C_f = C_{\rm forward}$). Experimental data of $C_{\rm rf}(V_g)$ curves are shown in Fig. 2 for different stress voltages always at accumulation. Only the curve before stress and the last one (after ten stress cycles) are shown for clarity. Usually, they are strongly peaked functions, going to zero above flatband or below inversion. However, in the data shown in Fig. 2, one peak lies in the depletion region (peak A), where, mainly, the interface traps respond, while another peak (peak B), in strong accumulation, appears in all curves. The deformation of the C–V_g curves in accumulation is commonly attributed to excess charge trapping in the oxide and is usually absent in state-of-art Si-based MOS devices. However, even in the case of a strongly peaked $C_{\rm rf}(V_g)$ function at depletion, this peak is due to both interface and bulk oxide traps. Therefore, the curves in Fig. 2 were deconvoluted in order to study, separately, the two kinds of traps. As shown in Fig. 2(a), peak A remains constant after CVS at low applied fields and a total stress time

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of 10 000 s, while peak B decreases. The result is reasonable for the peak due to the interface states; their density does not change after CVS at low fields. However, the reduction of peak B could be attributed to the capture of positive charges but this is impossible, as the MOS devices are biased in accumulation and the Ge substrates is n-type. The picture is completely different in Fig. 2(b), where the applied stress field is moderate (3 MV/cm); both peaks increase mainly because of the creation of new (interface and bulk) defects. Therefore, it is reasonable to assume that the reduction of peak B in Fig. 2(a) is due to the presence of relaxation effects in the oxide. This assumption is supported also from other measurements, as will be explained in the next paragraphs.

Some remarks must be made about the measurement procedure (as shown in Fig. 2 and the relevant text in the previous section) and the interpretation of the data obtained in this way. It is well known that trapping is a strong function of the applied field and that this can be understood as the result of equilibrium between the trapping/detrapping processes in the oxide. Moreover, when the stress is stopped, a redistribution of charges in the oxide is observed [37]. In this way, the trapped charge density measured during the monitor ramps cannot be considered as a direct measure neither of the trapped charge density during the high-field stress conditions nor of the generated trap density. Only an effective trap density is measured, which corresponds to the traps which are filled under the monitor conditions.

B. CVS at Moderate E_{ox}

The effective dielectric constant of the polycrystalline CeO_2 thin films was evaluated from the hf ($f = 100$ kHz) capacitance–voltage (C–V_g) characteristics of the MOS devices and was found to be around 25, in agreement with previously reported data on similar structures [13], [17]. Although the dielectric constant is quite high, the corresponding devices are rather leaky due to the low band gap of CeO_2($\sim$3.3 eV) in tandem with the small conduction band offset [5]. The current transport mechanism of the studied MOS devices is shown in Fig. 3. Due to the small conduction band offset, the leakage current in accumulation mode is due to thermionic (Schottky) emission at low to medium fields across the dielectric layer [39]. However, at higher fields, it is the Poole–Frenkel emission that controls the conduction through the oxide. The results shown in Fig. 3 have been confirmed, also in a series of similar structures with CeO_2 thicknesses ranging from 6 to 9 nm with temperature-dependent I_g–V_g measurements [40].

Figs. 4 and 5 show the current density change (ΔJ) during the application of a CVS pulse. The experimental data can be very nicely described by a model proposed by Nigam *et al.* [26], where ΔJ, as a function of time (t), is given by the following:

$$\Delta J = N^{+}(E_{\text{ox}}) \cdot \left[1 - e^{-\frac{t}{\tau}}\right] + \alpha \cdot t^{\nu} \qquad (2)$$

where $N^{+}(E_{\text{ox}})$ is the saturation value of positive charge trapping, τ is the trapping time constant, and α and ν are the SILC-related parameters, as discussed further on. The first term in (2) represents an exponentially saturating trapping of negative charges on preexisting oxide defects, while the second term represents the increase due to SILC generation.

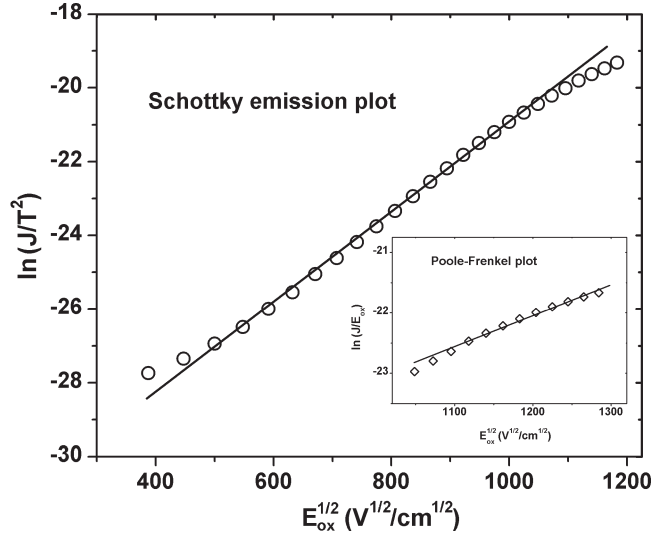

Fig. 3. Typical $J-E_{\text{ox}}$ curve of the devices showing thermionic (Schottky) emission at low to moderate E_{ox} values. The insert shows a Poole–Frenkel plot, as this mechanism dominates at higher E_{ox} values.

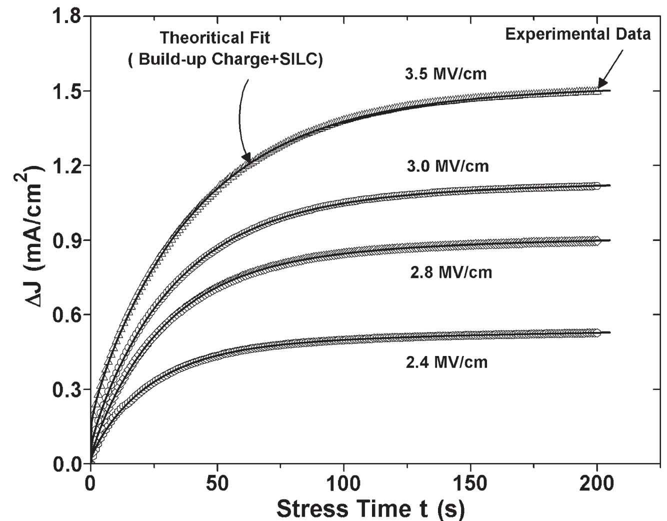

Fig. 4. Change of current density ΔJ observed during the stress time t under moderate to high stress field (CVS conditions). Symbols are experimental data, while solid lines are the best fit of both SILC and charge buildup, based on (3).

One difficult task in obtaining the necessary $\Delta J(= J - J_o)$ values from the experimental (J, t) pairs is the determination of the first value of the current density J_o. This value is actually equal to the leakage current of the device when no stress is applied. Small changes of J_o lead to a completely different slope of the curve and, therefore, an uncertainty in the fitting results, proving the necessity to determine J_o more accurately [41]. Fitting the actual current instead of the current change and treating J_o as a fit parameter can overcome this problem. In other words, (2) is rewritten as

$$J = J_o + N^{+}(E_{\text{ox}}) \cdot \left[1 - e^{-\frac{t}{\tau}}\right] + \alpha \cdot t^{\nu}. \qquad (3)$$

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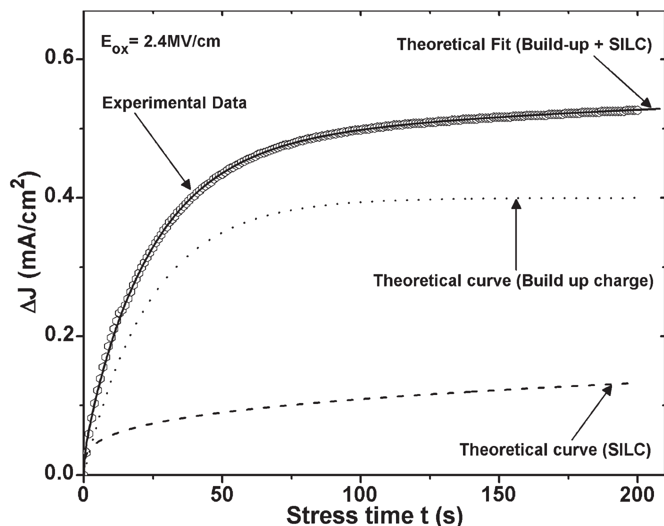

Fig. 5. Contribution of (dotted line) charge buildup and (dashed line) SILC to the total ΔJ versus t (symbols) experimental curve at 2.4 MV/cm. The solid line represents the summation of the two terms (SILC and charge buildup) based on (3).

Fig. 4 shows the absolute value of the measured current $|\Delta J|$ in the electric field $E_{\rm ox}$ range 2.4 MV/cm up to 3.5 MV versus time on a linear scale. The full line indicates the fit with (3). It should be noted here that, although the actual experimental data were fitted with (3), in Fig. 4, the ΔJ versus t curves are shown, as it is easier to study the trapping and SILC mechanisms with increasing applied stress field. The contribution of the two terms is shown in Fig. 5 for the case of applied stress bias $E_{\rm ox} = 2.4$ MV/cm. The charge-trapping component [the first term in (3)] clearly dominates as SILC is still not significant. Nevertheless, at higher fields, the experimental curve never reaches a saturation value because of the SILC component which becomes significant. Similar results have been found in SiO_2/Si-based devices [41], showing that the models used to explain oxide degradation are valid also in the case of Ge-based MOS devices. The most important difference in the case of a REO is that the charge-trapping component dominates over SILC in the entire field range (for applied stress fields from around 1.8 up to 4.0 MV/cm).

However, when intermediate or very low electric fields (from 0.5 up to 1.6 MV/cm) were applied during the CVS measurements, the results were rather complicated, as will be discussed in the next section.

C. CVS at Low $E_{\rm ox}$

Fig. 6(a)–(d) shows a set of $\Delta J, t$ curves for CVS conditions at $E_{\rm ox} = 0.8, 1.3, 1.5,$ and 1.8 MV/cm, respectively. It is interesting to notice that, at very low fields, CVS results in decreasing gate currents [Fig. 6(a) and (b)]. As there is no apparent source of positive charges when the n-Ge MOS devices are biased in accumulation, the realistic explanation is the presence of relaxation effects. These effects are expected to be detected in high-κ films when the leakage current is low. Therefore, a typical method for the estimation of the relaxation currents is to be measured after the sudden removal of a constant voltage on the gate [29]. However, this paper was focused on the investigation of charge-trapping mechanisms, and such a measurement was not done. This is the reason that the relaxation effects are so weak in Fig. 6(a) and (b) and no attempt was made to fit the experimental data with the Curie–von Schweidler law $(J \sim 1/t)$. Nevertheless, the effects were studied more carefully in similar devices, and results on $Pt/HfO_2/Dy_2O_3/Ge$ devices have already been published [42].

At these low fields and at room-temperature conditions, SILC effects are negligible, and an enormous amount of time is needed before a change in J can be observed. For example, it has been shown by Stathis *et al.* [43] that, for an oxide with this thickness and area of 5×10^{-4} cm^2, it takes approximately 300 years to reach breakdown at $|V_g| = 1.9$ V. In this case, therefore, it is impossible to reach breakdown at lower fields within a reasonable measurement time.

However, when the applied fields are greater than 1.8 MV/cm approximately, the current through the oxide is at least one order of magnitude greater, and the current transport mechanism changes from thermionic emission to Poole–Frenkel (Fig. 3) so that the high density of bulk oxide defects are responsible for the leakage current, thus masking all relaxation effects.

Finally, at applied fields between these two extremes (that is from 1.3 up to 1.6 MV/cm), the corresponding J–t curves are almost flat over the entire time interval, as none of the aforementioned effects clearly prevails.

D. Buildup Charges and SILC Coefficients

Figs. 7 and 8 show the fit parameters of (3) as a function of the applied electric field. The parameters shown in Fig. 7 are related to the negative charge-trapping behavior of the oxide. As shown in Fig. 7, the trapping time constant (τ) increases linearly with increasing applied field. Similar to the observations of Nigam *et al.* [26] and Xie *et al.* [44] on SiO_2/Si structures, it is the considerably smaller number of available oxide traps that makes the trapping time constant longer at lower fields. The corresponding τ values ($\sim$30 s) indicate neutral defects, as will be discussed later. At the same time, N^+ decreases with respect to the applied stress bias, which indicates that charge trapping becomes less important at higher fields. Another important observation is that the preexponential factor N^+ is almost six orders of magnitude greater than conventional Si/SiO_2-based devices [41]. This is probably due to the poor interfacial germanate layer, which is not eliminated after the conventional FGA treatment used in this paper.

As shown in Fig. 8, the SILC-related parameters are plotted against the applied stress bias. Since SILC is directly related to the trap generation in the oxide, particularly at low injected fluence, both α and ν provide information on the stress-induced trap generation [26]. α is the leakage current caused by the traps generated after $t = 1$ s, and ν is the trap generation rate. Both parameters (α and ν) increase with increasing field, showing that SILC becomes important at higher stress fields, as a consequence of the trap generation density dependence on the field stress applied during oxide degradation. Similar results have been reported on Si-based MOS devices with different dielectrics such as $\nu = 0.15$ to 0.30 on SiO_2/Si [26], [35], [41] and $\nu = 0.73$ on HfO_2/Si [45]. The calculated ν values for

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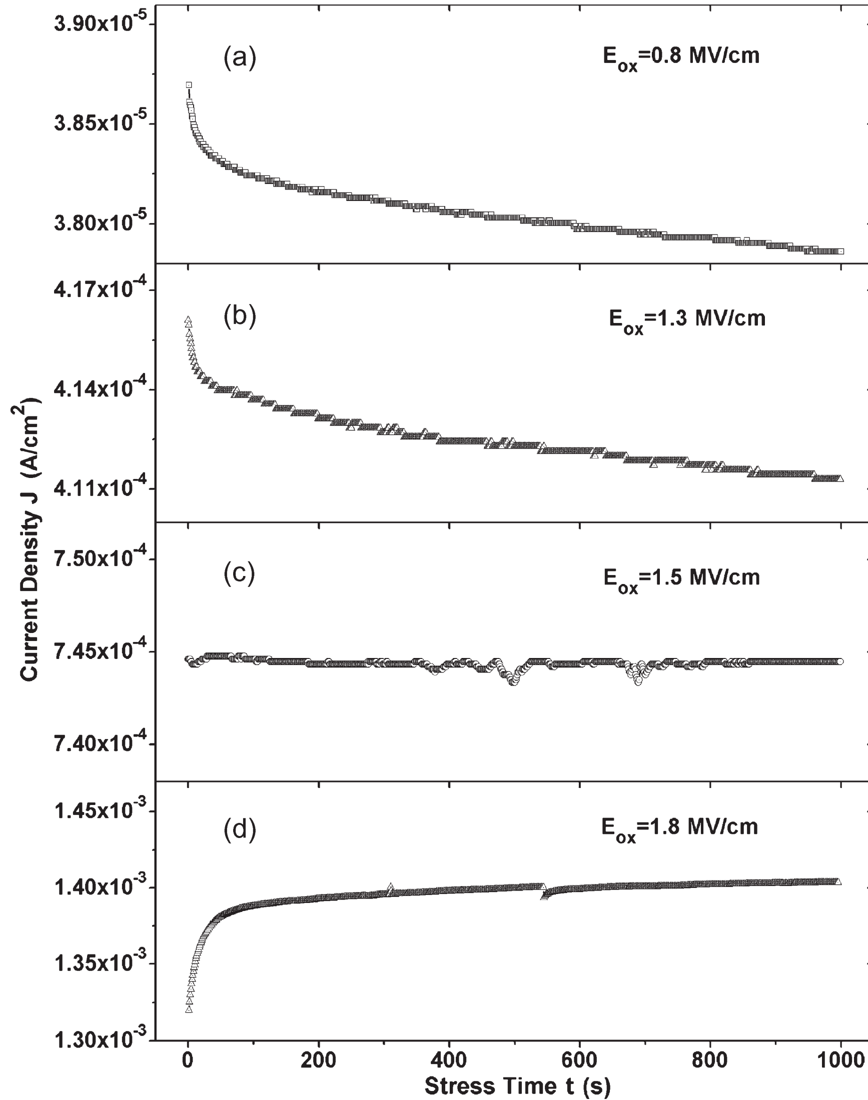

Fig. 6. Current density J as function of stress time t during CVS at lower stress field (0.8–1.8 MV/cm), showing relaxation effects for applied $E_{\mathrm{ox}} < 1.3$ MV/cm.

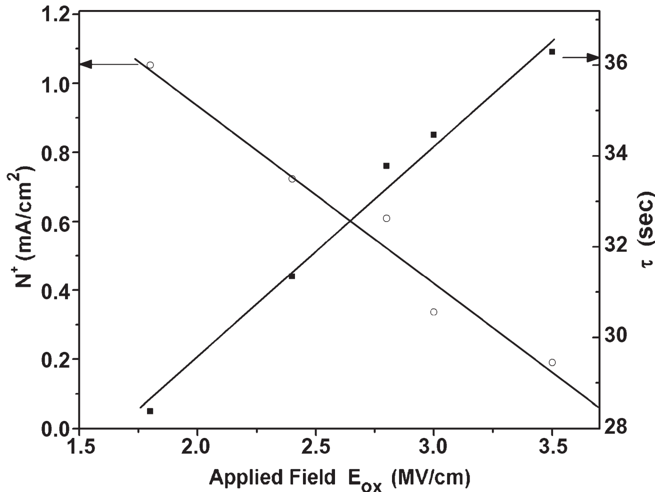

Fig. 7. Fit parameters (left axis) N^+ and (right axis) τ related to the charge buildup term as a function of E_{ox}. The lines are simply a guide to the eye.

a CeO_2/Ge system indicate that the choice of semiconductor substrate plays no important role in the mechanisms involved in SILC creation.

E. Capture Cross Section of Traps Investigated

The trapping time constant (τ) used in (3) is given by [46]

$$\tau = \frac{1}{\bar{\upsilon}\sigma_t n_e} = \frac{q}{\sigma_t J_g} \tag{4}$$

where $\bar{\upsilon}$ is the mean thermal velocity of electrons in CeO_2, which is considered approximately equal to the electron drift velocity; q is the electronic charge; n_e is the average injected electron density; and J_g the mean current density injected into the gate dielectric during the electrical stress, which is approximately proportional to n_e. The cross section of the traps (σ_t) is defined as the ratio of the capture probability to the thermal velocity of the electrons.

The time constant τ was extracted from the experimental curves shown in Figs. 5 and 6 using (3) and is shown in Fig. 9 as a function of $1/J_g$. It is observed that τ varies almost linearly with $1/J_g$, as predicted by (4); hence, the trap cross section σ_t was estimated from these data to be around 4.3×10^{-18} cm^2. Quite small values for σ_t have been also found in similar high-permittivity gate stacks grown on silicon (Si) substrates, as

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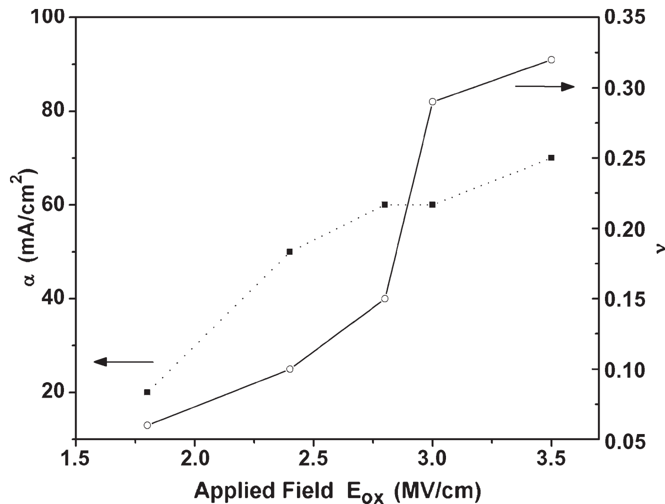

Fig. 8. Fit parameters (left axis) leakage current α and (right axis) trap generation rate ν related to the SILC as a function of $E_{\rm ox}$. The lines are simply a guide to the eye.

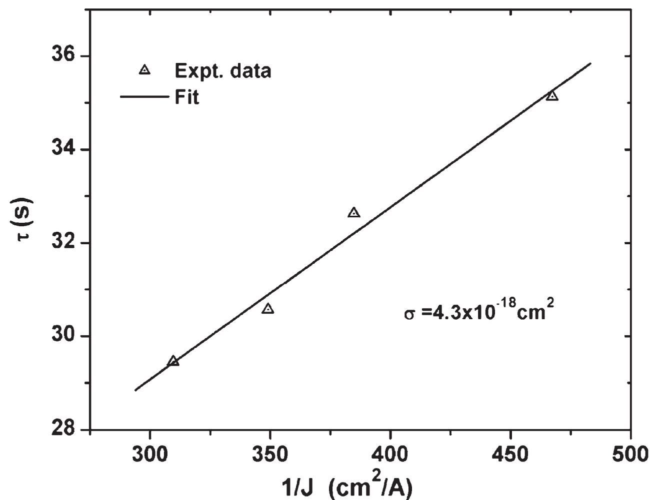

Fig. 9. Time constant τ as a function of the inverse current density $(1/J)$ injected into the gate dielectric during CVS at moderate stress fields. The capture cross section is obtained from the slope of the best fit line based on (4).

compared with values on the order of 1×10^{-16} cm^2 in SiO_2. These small values for the capture cross section suggest that the traps generated during the electrical stress are neutral centers [47], [48]. In the case of SiO_2, neutral trapping centers with cross section on the order of 10^{-16} cm^2 have been attributed [49] to SiOH centers generated during the release of H^+ by hot-electron impact ionization at the anode, followed by the breaking of bridging O bonds by these H^+ protons, which are subsequently trapped by the resulting SiO_2 sites. However, in the present case, this mechanism is not likely to happen, as the applied fields are not strong enough to create hot electrons.

IV. Conclusion

Thin cerium oxide layers deposited on Ge (100) substrates were subjected to constant voltage electrical stress in order to study some fundamental reliability issues of the corresponding devices. For stress fields higher than 1.8 MV/cm, it was observed that the contribution of the charge-trapping component has a significant impact on the measured curves while the effect of SILC component is faint. In the applied field range studied (1.8 up to 3.5 MV/cm), SILC generation follows a power law model similar to a number of works reported earlier on SiO_2/Si structures. The trap generation rate was found to be very small but rapidly increasing with increasing stress bias. These results are not surprising since the high-κ dielectrics currently studied are good insulators and suffer from the high density of both interfacial and bulk defects. Direct comparison of the N^+ and ν values of the MOS capacitors studied in this paper with SiO_2/Si-based systems is rather useless, as the latter suffer from SILC generation due to tunneling currents while trapping on preexisting defects is very small.

The effective cross section of the traps obtained from the analysis of the J–t curves was very small $(4 \times 10^{-18}\ \text{cm}^2)$, suggesting the presence of neutral traps. As the postannealing treatment in hydrogen environment (FGA) did not result in better (in terms of leakage current) devices, one can conclude that the main type of defects is oxygen vacancies, a common problem in high-κ dielectrics. Finally, a very weak relaxation effect was detected at applied stress fields lower than 1.8 MV/cm.

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