Anomalous charge trapping dynamics in cerium oxide grown on germanium substrate

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We have observed charge trapping phenomena in thin films of cerium oxide on *n*-type germanium (Ge) substrate under constant voltage stress (CVS) condition. The measured shift of the flatband voltage of a high frequency *C-V* curve immediately after each CVS cycle, was utilized as a method to study the capture dynamics of both preexisting and stress induced oxide defects. At low stress electric field, it is the creation of new interface traps that dominates the trapping characteristics of the corresponding metal-oxide semiconductor capacitors. At higher stress electric field, negative charges are trapped on preexisting traps uniformly located in the bulk of the oxide. From data analysis, the capture cross section of the traps is estimated to be around 1×10^{-19} cm^2 which indicates neutral traps possibly related to H^+ species and/or oxygen vacancies. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2901214]

I. INTRODUCTION

Charge trapping is a common phenomenon observed in most high-κ materials.[1–11] As a matter of fact, the use of dielectric layers with higher permittivity should allow us to use thicker films with equivalent electrical thickness than SiO_2, and one would expect to reduce charge trapping and the stress induced leakage current (SILC), thus improving the reliability of the corresponding device. In addition, germanium based metal-oxide-semiconductor (MOS) devices are currently extensively studied due to the high mobility of Ge.[5–9] One of the biggest challenges for the development of a Ge MOS technology is to find appropriate passivating materials and methodologies for the Ge/high-*k* interfaces. Germanium oxynitride (GeON) is frequently used as a passivating interlayer in combination with HfO_2 and is found to be necessary for the fabrication of functional devices.[12] However, it is also considered to be insufficient since electrical characteristics in capacitors are nonideal and field effect transistors underperform for reasons which are not fully understood at the present time, although the high density of interface defects probably play a role.

In a recent work, it was shown that cerium oxide (CeO_2) deposited directly on Ge by molecular beam deposition (MBD) reacts strongly with the substrate producing a thick interfacial layer which contain oxidized Ge.[13] Despite the Ge oxidation, this layer produces metal-insulator-semiconductor (MIS) capacitors with improved *C-V* characteristics as, for example, very weak frequency dispersion in depletion and inversion, small hysteresis, and much reduced density of interface states values ($D_{it}<10^{12}$ eV^{-1} cm^{-2}). Knowing that CeO_2 is a good catalyst, spontaneous formation of GeO_x or Ce–Ge–O interfacial layers is not surprising.

Charge trapping is a major device reliability issue since it causes flatband voltage shifts (V_{FB}) and drive current degradation over device operation time. It also precludes accurate mobility (inversion charge) measurements due to a distortion of *C-V* curves.[2,10] The charging is believed to be mostly due to trapping on preexisting defects in the high κ layer and its interface with the semiconductor. New traps can be created under certain condition (e.g., under high gate bias[14] or hot charge injection[15]). When the dielectric films have improved charge trapping characteristics, the corresponding MOS devices appear to have better electron mobility.[10] Charge trapping phenomena are well documented in the literature.[1–8] Additionally, although the relevant literature on Si based devices is rather rich, studies of Ge based structures are still limited. In the present work, we report on the trapping characteristics of Ge (100) based MOS devices with cerium oxide as the dielectric material.

II. EXPERIMENTAL PROCEDURE

Thin insulating films of CeO_2 were grown on *n*-type Ge (100) substrates using MBD. The CeO_2 layers were deposited directly on *n*-type Ge by atomic oxygen plasma beam from an e-beam evaporator. MIS capacitor structures were fabricated using a shadow mask so that the top gate contacts were deposited by Pt and the bottom Ohmic contact was made by eutectic In–Ga alloy. The thickness of the samples was estimated by x-ray reflectivity measurements to be approximately 10 nm. For postdeposition annealing, we used forming gas annealing (FGA: 95% N_2+5% H_2) to anneal the samples under various temperatures. For the present study, the CeO_2/n-Ge structures were annealed at 200 °C for 20 min. In a previous work,[16] it was shown that, forming gas annealing does not clearly improve the electrical characteristics of CeO_2/n-Ge MOS capacitors, showing similar or even higher leakage current after postannealing treatments. Nevertheless, for the samples used in the present study, forming gas annealing was beneficial in terms of a reduced leakage current. The MOS diodes were characterized electri-

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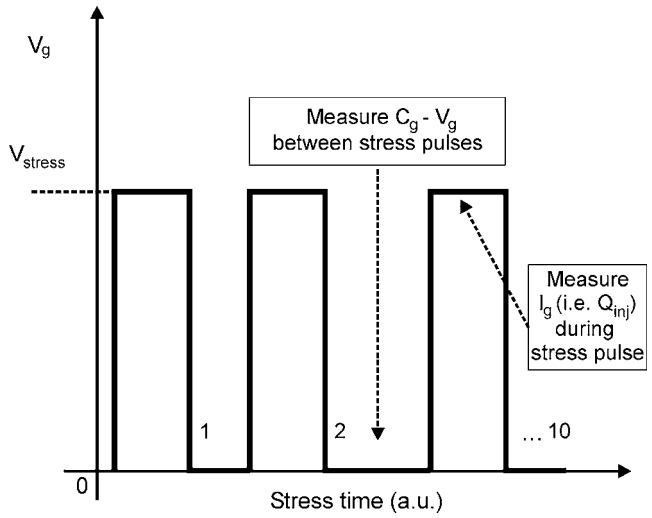

FIG. 1. Illustration of the pulsing technique used for charge trapping measurements.

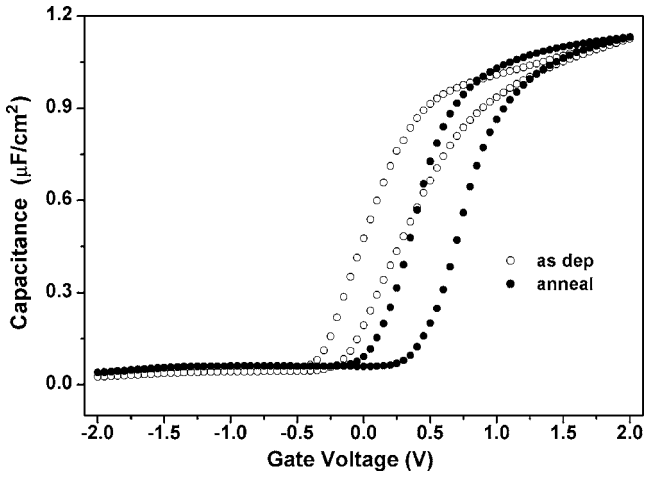

FIG. 2. *C-V* of as-deposited and annealed at 200 °C samples measured at $f=1$ MHz.

cally by means of capacitance-voltage (*C-V*), conductance-voltage (*G-V*), and current-voltage (*I-V*) measurements before and after annealing.

Consequently, the devices had been subjected to electrical stress under constant voltage stress (CVS) conditions, whereas the *C-V* and *I-V* curves were measured after each stress cycle using an Agilent 4284A *LCR* meter and a Keithley 617 electrometer. Charge trapping was studied by measuring flatband voltage shift (V_{FB}) of high frequency (100 kHz) capacitance-voltage (*C-V*) curves as a function of charging time (or injected charge) by using a pulsing (also known as "stress and sense") technique shown in Fig. 1. Fresh devices of area 7×10^{-4} cm^2 were used for each stress measurement. Finally, we note that the pulse duration used in our experiments was chosen to be rather long (500 or 1000 s) which is especially useful in order to investigate long-term V_{FB} instability and reliability phenomena.

III. RESULTS AND DISCUSSION

A. *C-V* and *I-V* measurements

Initially, the MOS devices were characterized by means of the analysis of conventional *C-V*, *G-V*, and *I-V* curves. Figure 2 shows the *C-V* characteristics of the films before and after annealing. A number of films have been grown at the same growth conditions with the physical thickness of the oxide d_{ox} (ranging between 7 and 14 nm) as the only changing parameter. Following a typical analysis for the evaluation of the equivalent oxide thickness (EOT) for each film and a plot of EOT versus d_{ox}, we obtained the dielectric constant of the ceria films ($\kappa_{ox}=23$).[13] While the calculated κ value is very good, the existence of a defective interfacial layer with physical thickness between 1 and 2 nm and a dielectric constant $\kappa_{il}=11$ was also obtained from the same plot.[17] This interfacial layer was also confirmed from high resolution transmission electron microscopy measurements.[13,16,17] This rather thick interfacial layer is probably the reason for the high density of oxide defects of the corresponding MOS devices and proper annealing treatments is currently under investigation in order to benefit from the high κ value of the ceria films after proper passivation of the Ge/Ceria interface. The existence of this layer will be also taken into account in the next paragraphs dealing with the trapping phenomena. It should be emphasized here that, in the present work, we report on the electrical characteristics and the related trapping phenomena of one set of samples with physical oxide thickness around 10 nm as mentioned before.

A comparison of the 1 MHz *C-V* curves in Fig. 2 shows a negative charge trapping after annealing in forming gas. When the flatband voltage shift is used to quantify the amount of trapped charge, it is the bulk oxide charge that is usually probed. On the contrary, when the width of the hysteresis loop is under examination, it is the amount of "border traps"[18] being investigated. The latter case will not be examined in this work. However, the amount of the bulk oxide trapped charge before and after annealing could be obtained from the high frequency (hf) *C-V* curves. The calculated value of $Q_{ot}(=\Delta V_{FB}C_{ox}=3.06\times10^{-7}$ C cm$^{-2})$ is rather high and reflects the poor quality of the semiconductor/oxide interface.

Figure 3 illustrates the current density as a function of applied bias for both as deposited and annealed samples. The current transport through the ceria film is due to the Schottky mechanism for low and medium fields (corresponding V_g in the range of 0–1 V) while at higher fields, it is the trap assisted tunneling (TAT) model[19] that best describes the experimental data. It is also obvious that the current density at $V_g=1$ V is quite high (around 1 mA/cm^2). This is consistent with previously published data on ceria films[20] which show that the high leakage currents are mainly attributed to the relatively small energy gap of the oxide ($E_g=3.3$ V). After annealing, the onset of TAT conduction moves to slightly higher gate voltages, which is consistent with a reduction of the amount of bulk oxide and interface defects. However, as the present work focuses on the trapping dynamics of the corresponding structures, we did not study the current conduction mechanisms with temperature in order to obtain more precise quantitative results.

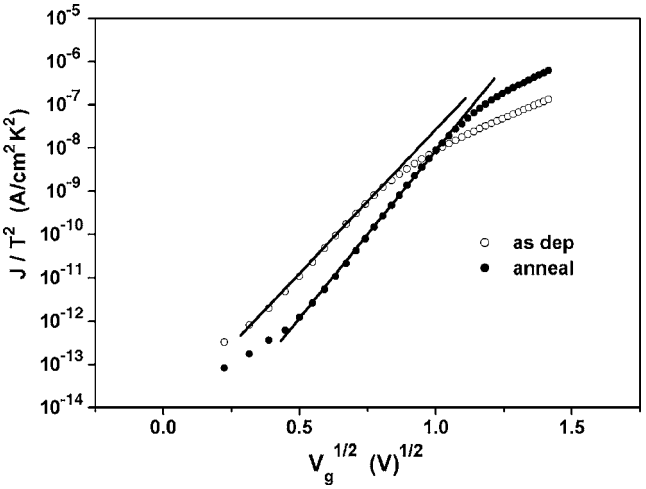

FIG. 3. Current-voltage characteristics of as-deposited and annealed $Pt/CeO_2/n$-Ge devices measured at $T=297$ K. The solid lines are simply guide to the eye for the Schottky-type current transport at low voltages.

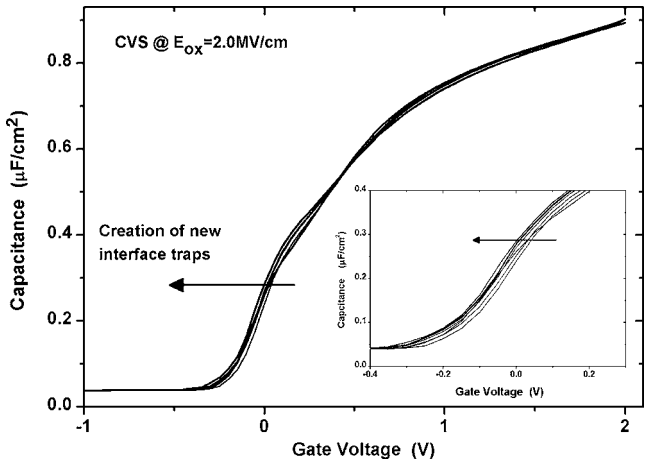

FIG. 4. High frequency C-V curves ($f=100$ KHz) of annealed films measured after CVS at a corresponding $E_{ox}=2$ MV/cm. The arrow indicates direction of flatband voltage shifts, ΔV_{FB} over time during stress. The inset shows an enlarged view of the curves around V_{FB} for the shake of clarity.

B. Constant voltage stress measurements

Only the annealed samples were stressed under CVS condition.[1,21,22] In general, the flatband voltage shift due to trapped charge in the oxide is given by[4]

$$\Delta V_{FB} = -\left[\frac{q}{C_{ox}}\right]\int_0^d \frac{x\Delta\rho(x)}{d_{ox}}dx, \tag{1}$$

where C_{ox} is the oxide capacitance, d_{ox} is the oxide physical thickness, x is the distance from gate electrode to trapped charge sheet, and $\rho(x)$ is the spatial charge density inside the oxide. The integral limits are taken from 0 to d_{ox} measured from the gate electrode. It is well known that a positive charge density results in a negative flatband voltage shift while the opposite is true for negative trapped charge.

Charge trapping was studied by measuring flatband voltage shift ΔV_{FB} of hf (100 kHz) capacitance-voltage (C-V) curves at various electric fields (ranging from 2.0 to 4.0 MV/cm) for a constant stress time interval equal to 1000 s. The applied voltages biased the devices at strong accumulation (i.e., injection of electrons from the germanium substrate), while all measurements were done at room temperature. Fresh diodes were used for each stress measurement (low field and high field). In Fig. 4, a negative flatband voltage shift ΔV_{FB} in the depletion region of the C-V curve is observed at the lower stress field used ($E_{ox}\approx 2$ MV/cm). This shift can be attributed to trapping at the interface states and is consistent with the corresponding "lowering" of the curves at strong accumulation. The so-called "stretch-out" effect is well known and a conventional analysis of the deformation of a hf C-V curve due to the presence of interface states can be found in any standard textbook.[23]

The study of the hf ac conductance versus gate voltage (G-V_g) measurements was then used as a tool to identify the location and/or the origin of the above-mentioned defects. Figure 5 shows the corresponding G-V_g plots for the devices stressed at a low ($E_{ox}\approx 2$ MV/cm) field, while Fig. 6 shows the evolution of the maximum G value (G_{max}) after each stress cycle for all three oxide fields studied. It should be mentioned here that the procedure followed for this experiment consisted of two steps: (i) application of a stress voltage at accumulation for a time interval of 500 or 1000 s and (ii) C-V and G-V measurement by sweeping the gate voltage from inversion to accumulation. In this way, all the trapping effects due to the application of a positive V_g were canceled whereas any new, stress induced interface defects could be detected by the change of the corresponding ac-G peaks. From Fig. 6, it is rather clear that the change of the G_{max} values at the lower stress field is initially twice as that of the higher E_{ox} stress values. After long stress times (5000 s), the discrepancy is minimized but the two high-E_{ox} curves never reach the lower E_{ox} one. This is a strong indication that the creation of new interface states dominates the trap kinetics at low oxide fields. It is also in perfect agreement with the explanation given for the stretch-out effect observed in Fig. 4 under similar CVS conditions.

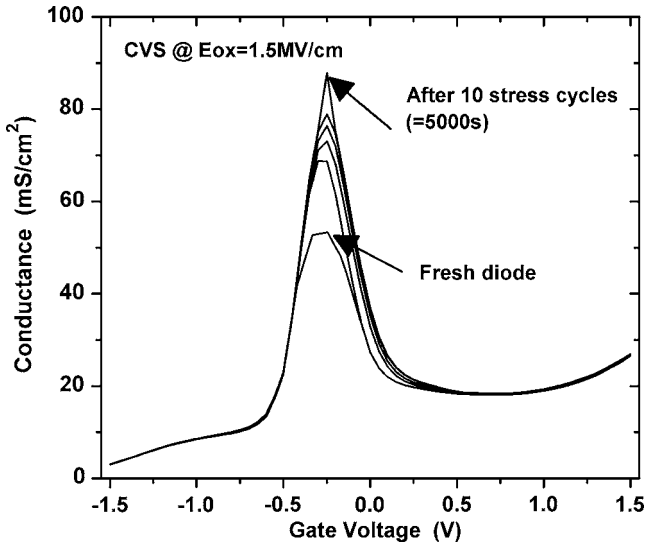

FIG. 5. G vs V_g curves ($f=100$ KHz) measured after CVS at a corresponding $E_{ox}=1.5$ MV/cm. Each curve was acquired after a 500 s long stress cycle. Not all data are plotted for clarity.

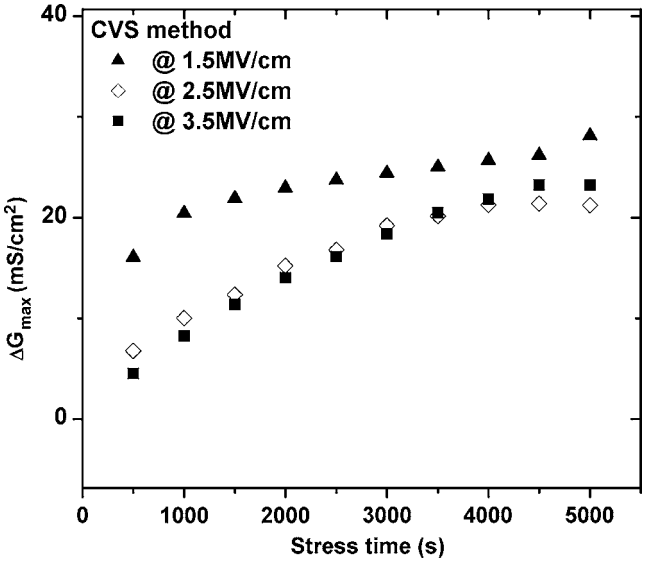

FIG. 6. Change of the conductance peak (ΔG_{max}) vs stress time (t) for different E_{ox} stress values.

On the other hand, at higher stressing field (E_{ox} >2.0 MV/cm) ΔV_{FB} becomes positive thus indicating the accumulation of negative charge in the oxide. As an example, the C-V curves at $E_{ox}=3.0$ MV/cm are shown in Fig. 7. This result is consistent with previously reported data on various gate stack combinations grown on Si or Ge substrates.[22,24] Also, it is consistent with electron trapping from the n-Ge substrate. It is interesting to note though, that in the accumulation region, the ΔV shift (the index FB does not apply in this case) is more pronounced than the ΔV_{FB} change in the depletion region. It is also more pronounced than the simple stretch-out effect we observed at low E_{ox} values (Fig. 4) and could be attributed to the high density of

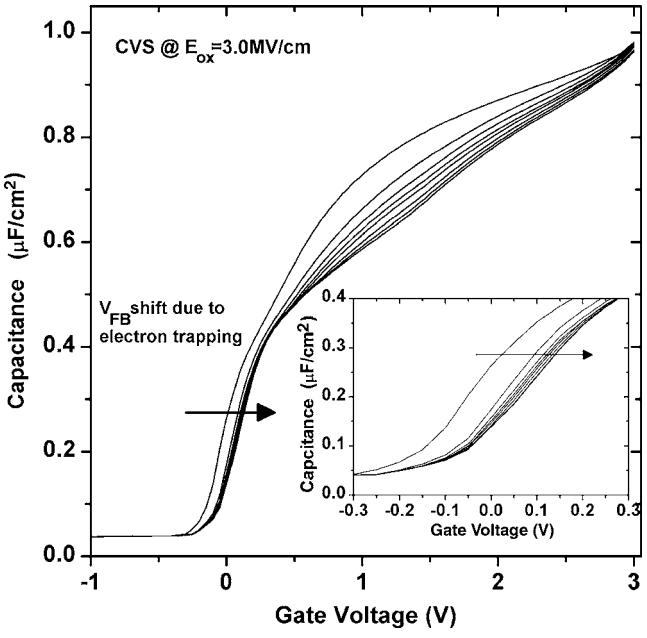

FIG. 7. High frequency C-V curves ($f=100$ KHz) measured after CVS at a corresponding $E_{ox}=3$ MV/cm. Positive shift of V_{FB} with stress time is observed as indicated by the relevant arrow. The inset displays an enlarged view of the curve around V_{FB}.

bulk oxide defects. A possible explanation for the positive ΔV_{FB} shift is given in the following paragraphs.

At low stress field values, the total trap density (neutral or charged) in the bulk dielectric (CeO_2) layer remain constant, whereas the stress induced flatband shifts are mainly attributed to the creation of new interfacial defects. The rate of creation of these defects will be discussed later in this section. However, at higher stress fields, the dependence of the voltage shift (ΔV_{FB}) on stressing time (t) can be expressed as[21]

$$\Delta V_{FB} = \Delta V_{max}\{1 - \exp[-(t/\tau)^{\gamma}]\}, \tag{2}$$

where ΔV_{max} is the maximum voltage shift, γ is an exponent which characterizes the distribution in capture cross sections, and τ is the time constant of the process, which is defined as[25]

$$\tau = \frac{q}{\sigma_i J_g}, \tag{3}$$

where q is the electron charge, σ_i is a characteristic capture cross section for the ensemble of traps with a continuous distribution of cross sections, and J_g is the mean current density injected into the dielectric during the electric field stress. Therefore, an equivalent approach to Eq. (2) is to describe the change of ΔV_{FB} as a function of the injected charge (Q_{inj}) as

$$\Delta V_{FB} = \Delta V_{max}\left\{1 - \exp\left[-\left(\frac{\sigma_i Q_{inj}}{q}\right)^{\gamma}\right]\right\}. \tag{4}$$

In the above equation, ΔV_{max} is directly related to the total oxide trap density. Exponent γ is also defined as a measure of the energy distribution of the traps and its value increases to 1 as the distribution width decreases to zero (i.e., one single level dominates the trapping characteristics). The injected charge is calculated from the fundamental equation:

$$Q_{inj} = \int_0^t J_g(t)dt. \tag{5}$$

In this case, the evolution of charge trapping with time is transformed to the dependence of the trapped charge as a function of the injected into the oxide charge from the semiconductor substrate. From J_g versus t measurements during CVS (not shown here for clarity), it was clear that the SILCs were very small, thus the J_g current was almost constant during the stress time intervals used in our experiments (t $=500$ or 1000 s) so, Eq. (5) reduces to the simple form: $Q_{inj}=J_g t$. The result of various stress fields on the ΔV_{FB} shift is illustrated in Fig. 8, where the negative shift at low E_{ox} values is clearly observed. The inset in Fig. 8 shows an enlarged picture of the same curve for $E_{ox}=2$ MV/cm in a log-log plot. The straight line that fits to the experimental data shows that the ΔV_{FB} shift follows a power law expression with respect to Q_{inj} which is given by[15]

$$\Delta V_{FB} = BQ_{inj}^{m} \tag{6}$$

The calculated value for $m=0.77$, lies in the range (0.3–1.0) as reported by many groups in the past irrespective of the substrate material chosen (Si or Ge).[24,26–28] This behavior

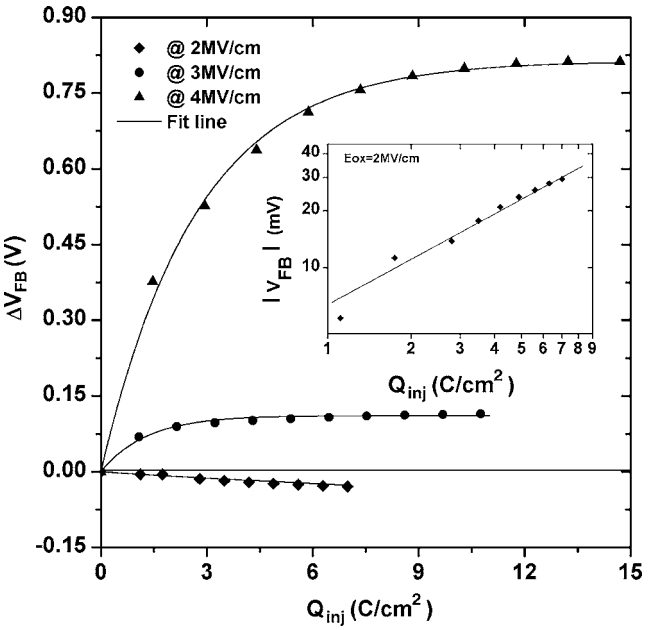

FIG. 8. Charge trapping monitored by flatband-voltage shift ΔV_{FB} of Pt/CeO_2/*n*-Ge as a function of injected fluence under various stress electric fields. Solid lines are best fit to experimental data according to Eqs. (4) and (6).

has also been observed on similar structures[15,22] and is, in general, attributed to the creation of new traps. Therefore, it is also consistent with the corresponding *C-V* and *G-V* curves (Figs. 4–6), as it was analyzed in previous paragraphs.

However, when the stress field (E_{ox}) is higher than 2 MV/cm, the situation is different. As shown in Fig. 8 ΔV_{FB} shifts are positive and they follow the exponential form of Eq. (4). The corresponding σ_i values are 1.3×10^{-19} and 0.6×10^{-19} cm^2 for $E_{ox}=3$ and 4 MV/cm, respectively. It is noticeable that for both fields, the experimental data are perfectly fitted by Eq. (4) with $\gamma\approx1$. In this case, Eq. (4) describes the filling dynamics of preexisting bulk oxide traps with a single capture cross section. From the small values for the capture cross section, it is inferred that the traps are neutral.[27] In addition, the decrease of σ_i with increasing stress field has been observed in neutral and Coulombic centers in SiO_2, HfO_2, and Al_2O_3 in the past.[21,22]

Therefore, we could argue that low stressing field (2 MV/cm) results in the creation of new interfacial defects thus distorting the corresponding *C-V* curves. When the capacitance at flatband condition is monitored, it seems to shift toward more negative V_g values. However, it is the stretch out of the hf *C-V* that is responsible for this effect. On the contrary, high stressing field ($\geqslant$3 MV/cm) results in a different conduction mechanism through the dielectric. The high density of electrons injected from the Ge substrate tunnel through the oxide defects so, we observe negative charge trapping on these defects. Finally, from the *C-V* measurements, it is inferred that at E_{ox} values as high as 4 MV/cm, the amount of new, stress induced oxide defects is undetectable and probably masked by the stronger electrical effect of charge trapping on the preexisting bulk oxide defects.

One important issue to understand is to what extent charge trapping in rare earth oxides grown on Ge substrates is intrinsic to metal oxides and how can this problem be cured. For example, Gusev *et al.*[29] studied HfO_2 layers deposited on silicon substrates with or without special interface preparation and they found that charge trapping does depend on interface quality. They have also shown that rapid thermal annealing in nitrogen environment is not sufficient to reduce these oxide defects. In a recent work[30] the authors suggest that the preexisting oxygen vacancies in HfO_2 based *n*-type MOS field-effect transistor can be cured by proper postdeposition annealing (reoxidation under proper conditions). Our results are in agreement with the above-mentioned studies, i.e., oxygen vacancies in rare earth oxides grown on Ge play a very important role in the charge trapping dynamics of the corresponding systems. The choice of different semiconductor substrates (Ge instead of Si) is not so important. It is the semiconductor/insulator interface quality that makes the difference. However, the common postdeposition annealing process for Si based devices in hydrogen (FGA) is not sufficient for the similar Ge based structures.

IV. CONCLUSIONS

In this work, charge trapping phenomena were studied in Ge based MOS structures with CeO_2 as the dielectric layer. All devices were initially annealed in forming gas at 200 °C in order to improve slightly their electrical characteristics. From our observations, we found anomalous charge trapping in the bulk of CeO_2 dielectric when the devices were stressed at accumulation (positive gate voltage on the gate electrode). At lower stress fields, the creation of new interface traps results in an observed negative V_{FB} shift which could be mistaken as an indication of positive trapped charge. Our experiment showed that this was not true; actually, it was attributed to the creation of an excess amount of new interface defects and the corresponding stretch-out effect on the *C-V* curves. On the contrary, negative charges (electrons) were trapped in the oxide at higher stress field. This was due to the enhanced current density through the oxide and the corresponding electron capture on preexisting bulk traps dominates over any interface related defect creation. The investigation of the trapping characteristics of the cerium oxide dielectric layer by means of analysis of the relevant flatband shift of the hf *C-V* curves could only provide information for the preexisting bulk defects. Their small capture cross section is an indication of neutral traps. These are possibly oxygen vacancies which have been also detected and studied extensively in various metal oxides grown on Si. Only interfacial, stress-related defects were identified at low stressing voltages, while no stress induced bulk defects could be detected. Therefore, a different postdeposition annealing process is needed if CeO_2 is to be used as an interfacial layer in future high-*k*/Ge MOS devices.

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