Gate stack dielectric degradation of rare-earth oxides grown on high mobility Ge substrates

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(Received 8 June 2012; accepted 3 October 2012; published online 1 November 2012)

We report on the reliability characteristics and their analysis, of rare-earth oxides (REOs) dielectric degradation, when used as interfacial buffer layers together with HfO_2 high-k films (REOs/HfO_2) on high mobility Ge substrates. Metal-oxide-semiconductor (MOS) devices with these stacks, show dissimilar charge trapping phenomena under varying levels of constant-voltage-stress (CVS) conditions, influencing the measured densities of the interface (*Nit*) and border (N_{BT}) traps. In the present study, we report on C-V_g hysteresis curves related to both *Nit* and N_{BT}. We propose a new model based on the Maxwell-Wagner mechanism, and this model explains the current decay transient observed under CVS bias from low to higher fields of MOS gate stack devices grown on Ge substrates. The proposed model is unlike to those used for other MOS devices. Finally, CVS measurements for very long times at moderate fields reveal an initial current decay due to relaxation, followed by charge trapping and generation of stress-induced leakage which eventually lead to hard breakdown. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4763478]

I. INTRODUCTION

Rate-earth oxides (REOs) such as CeO_2, Dy_2O_3, and La_2O_3 are used for the construction of gate stacks on Germanium substrates demonstrating excellent passivation of the surface and electrical properties.[1] However, it is important to clarify a number of reliability concerns such as, charge migration at the interface of the two dielectrics, charge trapping inside the bulk of the oxides, defects generation under bias, stress-induced leakage current (SILC), and oxides degradation issues. One of the serious drawbacks in most of the high-k dielectrics is the charge trapping in the bulk of the oxides. This precludes accurate extraction of mobility, flatband (threshold), and voltage shift ($V_{FB/th}$) while it also results in the degradation of the device electrical characteristics.

When MOS capacitors (MOSCAPs) are stressed under pulses of constant gate voltage, the flatband voltage (V_{FB}) is extracted from capacitance-voltage (C-V_g) or current-voltage (J_g-V_g) measurements taken between the pulses. This is monitored as a function of either the stress time or the injected charge while the leakage current is recorded simultaneously. During the measurements, a good setup is maintained to avoid the influences of external charging/discharging effects to the built-in defects within the dielectric itself. It has to be noted here that even little C-V_g (or J_g-V_g) hysteresis can significantly affect the outcome (instability).[2]

The bulk or interfacial defects give rise to transient gate currents while it has widely been accepted that the defects existing in high-k dielectrics play an important role when the devices are in operation.[3] Moreover, during a stress bias, new neutral defects/traps are created in the oxides. Depending on the stress conditions this creation of the new defects affects the resultant external leakage current. SILC is the signature of the defect generation within the gate stacks, and it is independent of the dielectrics in the stacks. The continuation of the charge trapping and defect generation leads to dielectric degradation and eventually causes hard breakdown (HBD) of the devices.[3] SILC is not only related to the generation of new defects but results also from the localized, defect related weak spots near the injecting interface.[4,5] The newly generated traps are uniformly distributed in the bulk of the oxides. Moreover, the interface traps play a crucial role on the dielectric degradation and the electrical instabilities.[6] In high-k dielectrics, the gate stack itself causes charge accumulation and exhibits a decay current transient behavior. This current decay behavior can be explained by means of the so called Maxwell-Wagner (M-W) instability,[7] named as one of the major drawbacks of gate stack technology since it hinters the passivation quality of the high mobility substrates surface, e.g., Ge.

Another class of oxides defects, were introduced and termed by Fleetwood as "border traps," or "near interface oxide traps (NOIT)."[8] These border traps exchange charge with the semiconductor substrate on the time scale of the measurements being performed.[9] This charge exchange is typically slower than that of the interface traps, so sometimes these defects are called "slow states."

As the MOS devices continue to scale down rigorously, the influences of the interface and the border traps on device performance and reliability become more important.

When charges are accumulated at the interface of the bilayer dielectrics, this situation accelerates the relaxation polarization due to the different conductivities of the dielectric materials. Dielectric relaxation follows the direction of

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the applied external voltage gradient (dV_g/dt) when devices are under bias constant-voltage-stress (CVS). The simultaneous effects of the charge migration at the interface and the relaxation polarization of the multilayer gate stacks cause the Maxwell-Wagner instabilities (M-W).[7] This relaxation behaviour is observed in very low level external circuit current regime, however at medium or higher bias the situation is different and includes charge trapping and creation of new neutral bulk oxide defects. When an external field is applied across a film, it separates the bound charges, thus resulting in polarization and a compensating internal field.

In this paper, we are dealing with the electrical reliability characteristics of rare-earth oxide based gate stacks (REOs-HfO_2) in a step by step way using long CVS dielectric degradation of Ge based MOS devices.

II. EXPERIMENTAL

Thin films of REOs/HfO_2 oxide stacks were prepared by molecular beam deposition (MBD) on both *p*- and *n*-type Ge (100) substrates. The REO used were Dy_2O_3, La_2O_3, and CeO_2. Native oxide was desorbed in situ under ultra high vacuum (UHV) conditions by heating the substrate to 225–360 °C for 15 min until a (2×1) reconstruction appears in the (RHEED) pattern, indicating a clean (100) surface. Subsequently, the substrate was cooled down to 225–336 °C, where the oxide stacks were deposited. The surface was exposed to atomic O beams generated by a radio- frequency plasma source with simultaneous e-beam evaporation of RE/HF at a rate of about ~0.15 Å/s. Metal–insulator–semiconductor capacitors were prepared by shadow mask and e-beam evaporation of 30-nm-thick Pt electrodes to define circular dots of 200–800 μm in diameter. The back ohmic contact was made using eutectic InGa alloy. The further experimental (deposition techniques, characteristics) details on CeO_2, Dy_2O_3, and La_2O_3 have been described in detail and elaborately in our previous work[1,6,13,18,23,28] together with their corresponding gate stacks with HfO_2 on Ge.

The devices were subjected to electrical stress under CVS conditions at accumulation using a Keithley 617 source/meter, and the same instrument was used for measurements of the current for successive stress cycles versus time (J_g-t) and the current–voltage ($Jg–Vg$) curves. The C-V_g curves at high frequency (100 kHz) were measured with an Agilent 4284 A LCR meter, more details can be found elsewhere,[7,10] All measurements were performed in a dark box and at room temperature. The advantages of using the MBD technique for growing the devices under test have been explained in previous work.[11,12] The main reason behind this choice over other similar techniques is the good stoichiometry obtained for the grown films. This assures us that the observed degradation mechanisms are affected by stoichiometric defects in a minimal way.

III. RESULTS AND DISCUSSIONS

A. C-V_g characteristics of Ge-based devices: anomalous trapping behavior

Fig. 1 shows the $C–Vg$ curves for low and medium CVS on MOS devices structured as: Pt/Dy_2O_3/*p*-Ge, respectively. The curves are recorded on fresh samples under forward and reverse bias sweeps with a gate voltage sweep rate of 50 mVs^{-1}, and after 10 successive stresses of 500 s each (i.e., $t_{stress} = 5000$ s). For the shake of clarity only fresh and after 5000 s CVS biased C-V_g curves are plotted in Fig. 1. However, the increasing trend of ΔV_{FB} (i.e., C-V_g curve shifts towards positive or negative direction, respectively) is observed consecutively with respect to the progress of each stress time.

The flatband voltage shift (ΔV_{FB}), which is related to the charge trapping in the devices, show both positive and negative ΔV_{FB} shifts at the same bias polarity. In the present case, the *p*-type Ge substrates supply holes at accumulation and we expect hole trapping (see Fig. 1(b)) inside the dielectric which will be uniformly distributed either in the bulk of the oxide or at the interface. However, Fig. 1(a) depicts unusual charge trapping characteristics on the C-V_g curves. This could be attributed to the fact that the gate bias is always negative at accumulation hence electrons from the gate are injected into the dielectric and captured by the preexisting traps. Nevertheless the applied field (E_{Dy2O3} ~2 MV/cm at

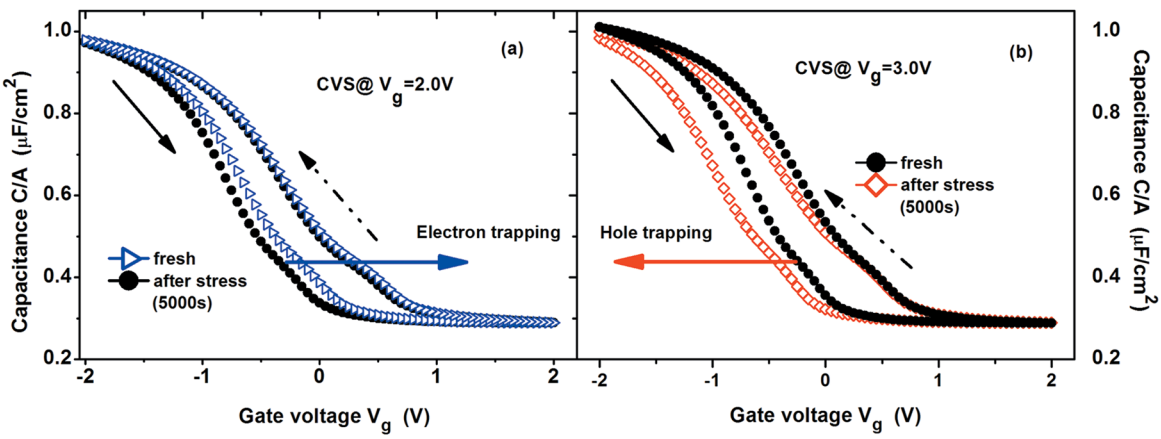

FIG. 1. (a,b) High frequency C-V_g ($f = 100$ kHz) curves on fresh and stressed devices of Pt/Dy_2O_3/*p*-Ge. Only the fresh curves and those after the application of ten consecutive CVS cycles (500 s each) are plotted for clarity. Stress voltage is low in (a) and moderate in (b). However, the increasing trend of ΔV_{FB} (i.e., C-V_g curve shifts towards positive or negative direction, respectively) is observed consecutively with respect to the progress of each stress time. Positive V_{FB} shifts in (a) indicate trapping of electron in the bulk of the oxides while negative V_{FB} shifts in (b) indicate creation of positively charged defects.

$t_{stress} = 0$ s) is not high enough to force the electrons escaping from the defects and driving them towards the substrate.

Structural measurements, e.g., Transmission Electron Microscopy (TEM) and X-Ray Reflectivity (XRR) measurements[13] showed that an additional ultrathin layer of GeO_2 was formed as an interfacial layer (*il*) with a lower value of the dielectric constant ($k \sim 5$) which finally worked as a gate stack structure. The aforementioned unalike charge trapping change of sign at accumulation could also be happening due to the dissimilar conductivities of the bilayer insulating films. This effect has been observed as a switching of the trapped charge sign when varying the gate voltage.[14] Another possible reason could be the different relaxation behavior of each layer in the gate stack.[15] Recently published work also suggested that this particular nature of charge trapping is, due to both relaxation and Maxwell-Wagner instabilities (M-W).[7,15]

The typical trapping phenomenon has also been observed for other REOs used in gate stack MOS devices,[7,10] and at the current moment is not well-understood. We also emphasize here that a large hysteresis of the C-V_g curves (see Fig. 1) is observed for Ge based MOS devices,[13,16,17] due to either the intermixing of the high-k and the interfacial layer, or to an excess amount of positive charges in the bulk of the gate stacks dielectric.

B. Border traps characteristics in REOs and its gate stacks

Our previous results, e.g., TEM and X-ray Photoelectron Spectroscopy (XPS),[18] showed that when CeO_2 was directly deposited on high mobility Ge substrates, it interacted strongly with the substrate and spontaneously formed a $1 \sim 2$ nm thick interfacial layer thus leading to a gate stack structure. Fig. 2 shows the C-V_g curve (circled symbol-line) and its hysteresis characteristics (solid line) of a CeO_2 based MOS devices. The measurement frequency was 100 kHz at a ramp rate of 50 mV/s, and the switching time for one complete hysteresis was 40 s.

The difference in C-V_g hysteresis from reverse to forward bias direction ($= C_{rf}$ [$= C_r - C_f$]) can be used to estimate the border traps (ΔN_{BT}).[8] The indexes refer to measurements from accumulation to inversion ($C_r = C_{reverse}$) and inversion to accumulation ($C_f = C_{forward}$). In the present case, this border traps estimation (ΔN_{BT}) is not similar to the one appearing at the classical Si/SiO_2 MOS devices where always a single peaked ΔN_{BT} curve is observed.[8] Fig. 2 depicts a double peaked curve, with peak "1" appearing at weak depletion and close to flatband region, and peak "2" appearing at accumulation; these two peaks can be attributed to contributions from interface and border traps, respectively.[10] The enlarged picture of the ΔN_{BT} is shown as an "insert" in the graph. At point "A" of the C-V_g curve we can eventually observe a "bump," which indicates the contribution of the interface traps to the C-V_g measurements. Hence both the bump at "A" and peak "1" correspond to interface traps, whereas peak "2" corresponds to the border traps as happens for the Si-SiO_2 system.[8] Similar results are also observed in other REOs based MOS devices grown on Ge substrates.[17,19]

As mentioned before, there are two types of border traps, the slow and the fast ones. A slower border trap will be counted in the C-Vg measurement as a bulk-oxide trap, unlike a faster one which will be counted as an interface trap. This results to the picture of the two peaks appearing at the ΔN_{BT} curves.

Fig. 3 shows the capacitance-voltage(C-Vg), conductance–voltage ($G_{p/\omega}$-V_g), and border traps estimation curves (ΔN_{BT} vs V_g), all in one graph, for the shake of clarity and understanding. A measure of the total effective border trap density (ΔN_{BT}) can be obtained by integrating the absolute value of the difference (C_{rf}) between the C–Vg curves, using the expression:[8,17]

$$\Delta N_{BT} \frac{1}{qA} \int |C_r - C_f| dV \tag{1}$$

where q is the elementary charge and A is the area of the MOSCAPs. The $G_{c/\omega}$-V_g was subjected to series resistance effect correction[20] and all data are normalized to area.

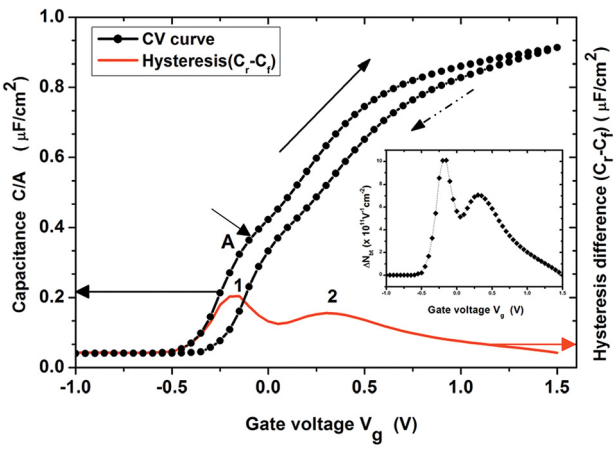

FIG. 2. The C-V_g curve (circled symbol-line) at higher frequency (100 kHz) and its hysteresis difference ($C_{rf} = C_r$-C_f) characteristics (solid line) of a CeO_2 based MOS devices. The double-peaked C_{rf} structure corresponds to interface and border traps at deep depletion and accumulation bias region, respectively, and the enlarged double-peaked curve is shown as insert in the figure for clarity.

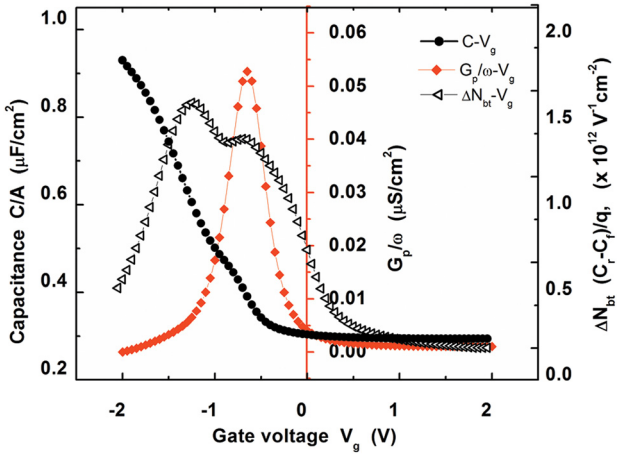

FIG. 3. The capacitance-voltage (C–V_g), conductance–voltage ($G_{p/\omega}$–V_g), and the estimation of border traps (ΔN_{BT} vs V_g) curves, all in one graph. The bump in the C–V_g curve (because of interface defects) and the $G_{p/\omega}$ peak (representing the losses due to the exchange of carriers with interface traps) show one-to-one relation with the second peak of the C_{rf} curve. Thus graph also confirms the additional peak due to N_{it} contribution to the C_{rf} curve from the Border traps analysis.

The "first" peak at the depletion region of the ΔN_{BT} vs. Vg curve and also the "peak" of the G_c/ω-Vg curve are one-to-one correlated. The corrected (G_c/ω–Vg) curves are strongly peaked at depletion, representing losses due to the exchange of carriers with interface traps.[20]

We can observe here that the additional peak at the C-V_g difference hysteresis curve (C_{rf}) hinters the interface traps contributions. This effect is known as "screening" and it is common in dielectrics other than SiO_2 on Si.[9,20]

Fig. 4 shows another experimental fact and convolution the border traps with respect to the time progress during CVS. If we itemize the evaluation of the N_{BT} under the CVS measurements it is noticeable that with respect to CVS biasing and with progressing stress time, the border traps continue to accumulate and the shape of the C_{rf}/q-V_g curves is changing dramatically, suggesting that the total amount of N_{BT} is increasing. This is well illustrated in Fig. 4 where the black solid-square line results from fresh devices and the red open-circle line is the ΔN_{BT} after stressing the device at a CVS of -2 V for $t_{stress} = 500$ s. The two peaks "A" and "B" in this case, represent the interface and border traps contributions to the C-V_g hysteresis curve[17] mentioned earlier. It is clear that during the stress conditions new defects are created continuously. Analyzing the above results, the total calculated amount of N_{BT} on both fresh and after stressed devices are equal to $3.1 \times 10^{12}\,eV^{-1}\,cm^{-2}$ and $3.96 \times 10^{12}\,eV^{-1}\,cm^{-2}$, respectively.

It is important to mention here that due to the difficulty to distinguish between the border and the interface traps, different groups have reported various opinions and procedures,[4,9,20–22] on this issue. These opinions refer either to the contribution of the surface passivation which may alter the physical nature of the defects, or to the fact that the defects density depends on the oxide processing, or both. The REOs are strongly reactive with Ge and during the deposition, the Ge molecules diffuse into it and this intermixing of the Ge and REOs could result to the above mentioned facts.[18] Earlier work on the passivating properties of REOs films showed better electrical quality for the La_2O_3 as compared to CeO_2 and Dy_2O_3,[18,23] and it is reported that when the interfacial layer of La_2O_3 was about 1 nm then the La_2O_3 or its gate stack (HfO_2/La_2O_3) did not demonstrate any additional bump in the C-Vg hysteresis measurement compared with those of CeO_2, Dy_2O_3, and also their gate stacks.[24]

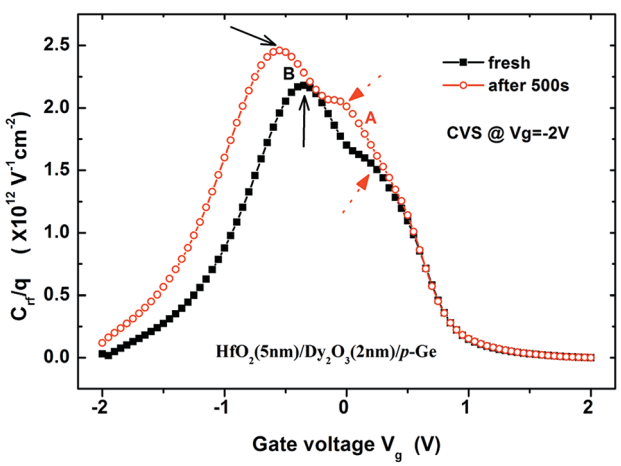

FIG. 4. Illustrates the evolution of "border traps" in Dy_2O_3/HfO_2 gate stacks under CVS conditions. Total number of "Border traps" increases with the progress of time (stress time, 500 s) during CVS in gate stacks which are equal to $3.1 \times 10^{12}\,eV^{-1}cm^{-2}$ and $3.96 \times 10^{12}\,eV^{-1}\,cm^{-2}$, respectively.

C. Interface traps, border traps, and oxides traps

C-V_g measurements at various CVS bias conditions and frequencies were performed in order to estimate the oxide (N_{ox}), interface (N_{it}), and effective total border traps (N_{BT}) densities. Devices with different thicknesses REOs gate stacks (REOs/HfO_2), were used, and the results are shown in Figs. 5(a) and 5(b) for low (-2 V) and high (-4 V) CVS biases and for 10 consecutive stresses of 500 s each (total $t_{stress} = 5000$ s), respectively. At low CVS the interface traps density is increasing almost exponentially with respect to the stress time but the border traps and oxide traps densities remain almost unaltered. The interface traps density is about one order of magnitude higher than the densities of the border and oxide traps.

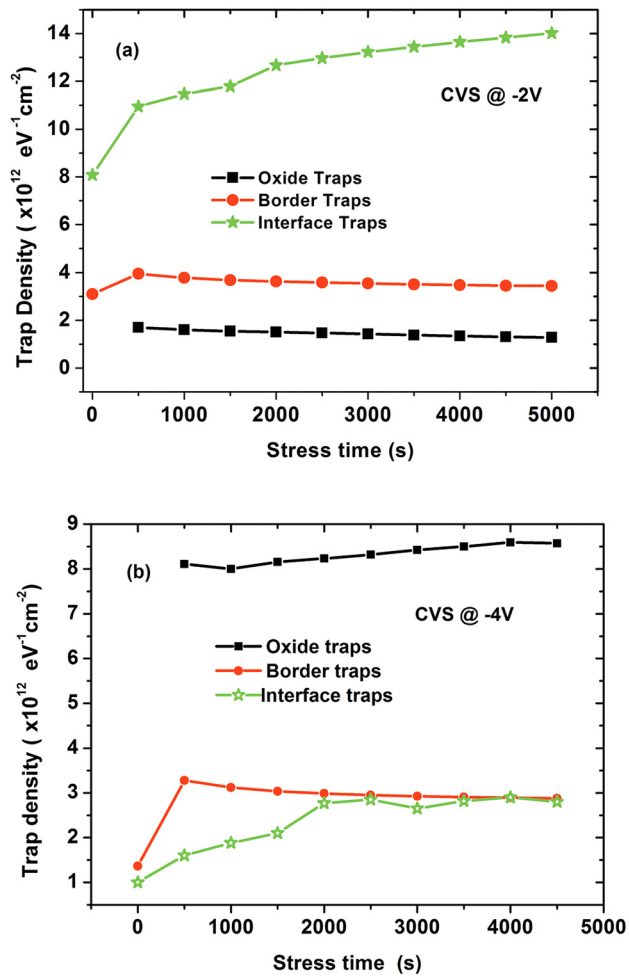

FIG. 5. The evolution of oxide traps (N_{ox}), border traps (N_{BT}), and interface traps (N_{it}) of Dy_2O_3/HfO_2 gate stacks at different CVS of low (-2 V) and moderate (-4 V) under 10 successive stresses of 500 s each, respectively. At low CVS, the N_{it} density is increasing almost exponentially and one order of magnitude higher with respect to N_{ox} and N_{BT} in stress time while at higher bias N_{ox} shows the similar behavior i.e. N_{ox} is increasing. These results also supports with the phenomena are observed in Figs. 1(a) and 1(b), respectively.

This increase of the interface traps density at lower CVS which could hinter the positive ΔV_{FB} shift (see Fig. 1(a)) also contributes to the ΔN_{BT} curves ambiguity (Figs. 2 and 3). At higher CVS conditions the device behavior is different but as usual characteristics (see Fig. 1(b)) of MOS devices.

The oxide traps increase for almost one order of magnitude, compared to that of the interface and border traps, is in agreement with the results shown in Fig. 1(b). The oxide traps create fixed defects in the bulk, which contribute to the large hysteresis in the C-V_g measurements appearing in Fig. 1. At higher biases the interface traps density (N_{it}) is also increasing but its value remains much lower than that of N_{ox}. In both cases, the border traps remain either flat or slightly increasing.

Similar results[24] have been reported in the past for CeO_2/Ge MOS devices with anomalous charge trapping, for same polarity stressing, due to the creation of new interface defects at low CVS. This is the distinct feature of the REOs grown on Ge substrates over Si-based MOS devices.

The N_{it} was calculated using a Ge-based simulator (MISFIT[25]) which solves both Poisson and Schrödinger equations simultaneously, taking into account quantum confinement effects, while the border traps were calculated, according to Eq. (1) and the oxide traps by using the methodology of reference.[10,24] The extraction of N_{it} from the high frequency C-V-G measurements of the Ge-based MOS devices is not an easy task, alike that of Si based MOS devices, when the conductance method is used. Batude *et al.* reported that this calculation overestimates N_{it} by almost one order of magnitude in Ge-based MOS capacitors,[26] however Bellenger *et al.* suggested contrary.[16]

D. J_g-t decay transients: current instabilities

The use of REOs as a buffer interfacial layer (*il*) demonstrates better passivation and electrical properties compared to other *il* layers between high-k (e.g., HfO_2, ZrO_2) and Ge surface itself.[6,18,27,28] However, in terms of reliability, when gate stacks of high-κ dielectrics are used in MOS devices they produce current decay behaviour, (decay transient of J_g-t) which is defined as Maxwell-Wagner instabilities (M-W).[7,15,29]

This M-W model, can explain the experimental results (J_g-t) under certain limitations: (a) until a certain stress time (i.e., $t_{\text{stress}} \leq 100$ s) (b) when the M-W current (J_{MW}) is very low and dominated mainly by the so called Curie-von Schweilder (C-S) relaxation current (c) at low CVS regime.[7] On the contrary, at low- to medium and certainly at higher CVS, new neutral defects/traps will be created[5,30–33] which give rise to SILC which is not included in that model. The creation of the neutral defects is defined as

$$J_{SILC} = \alpha.t^{\nu}, \tag{2}$$

where α is the pre-factor (in A/cm^2) and the power ν is the trap generation rate under a certain bias condition. Therefore, if we combine these $J_{M\text{-}W}$ and J_{SILC} components they result to a total external circuit current as

$$J_{(MW,SILC)} = J_{MW} + J_{SILC}, \tag{3}$$

$$J_{(MW,SILC)} = 2E_{h-k}\sigma_{0,1}\left(3 + \ln\frac{t}{t_{0,1}}\right)\frac{t_{0,1}}{t} + \alpha.t^{\nu}, \quad t > t_{0,1} \tag{4}$$

where E_{h-k} is the field across the main high-k dielectrics (here the HfO_2, so E_{HfO2}), $\sigma_{0,1}$ and $t_{0,1}$ are material constants which have the dimension of conductivity (A/cm^2) and relaxation time distribution (s), respectively. The value of $t_{0,1}$ is expected to be of the order of picoseconds.[7,15,29]

Using Eq. (4), a best fit to the experimental data (J_g-t) is obtained and clearly explains the results[7] (see Fig. 6). In the literature, the decay transients (J_g-t) have been described by various models: (a) a field lowering model due to charge trapping at the traps near the gate,[34] (b) a model using the C-S dielectric relaxation mechanism,[35,36] and (c) the M-W mechanism.[7,15,29] In our case, the new proposed model for the current instabilities explains very well the experimental results.

E. Time dependent dielectric degradations (gate stacks)

Finally the devices on both p- and n- type Ge substrates have been subjected to very long CVS conditions at moderate gate voltages. Fig. 7(a) shows the results for devices grown on p-type Ge-substrates and subjected to CVS at $V_g = -3.0$ V ($E_{HfO2} = 3.3$ MV/cm, $E_{Dy2O3} = 5.9$ MV/cm). Initially, the fit (C-S relaxation $J \sim t^{-n}$) to the J_g-t decay (first part) gives the n value as $n \sim 0.56$ while the charge trapping as described by Nigam *et al.*[17] is considered for best fitting of the experimental data shown in the second part, where the time constant, τ was found to be equal to 260 s. This device reached hard breakdown after a number of soft breakdown events and a total stress time in the range between 15 000 s and 20 000 s.

This result can be explained considering that one of the oxides (probably the thinner, 2 nm Dy_2O_3) goes to breakdown first, leading to a major redistribution of the corresponding fields. Thus, the field across the other dielectric

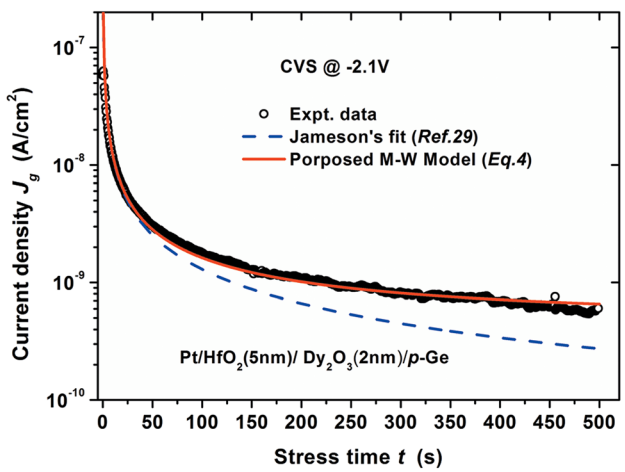

FIG. 6. It shows gate current as a function of stress time of gate stack (HfO_2/Dy_2O_3) semi-log plot. The dotted (blue) and solid (red) lines are fits, according to Eqs. (3) and (4) to the experimental data. The proposed model Eq. (4) for current instability (J_g-t transient), the M-W effects together with SILC explains completely the experimental data while previous models (Refs. 7 and 29) were unable to fit the data completely (but the first 40 s).

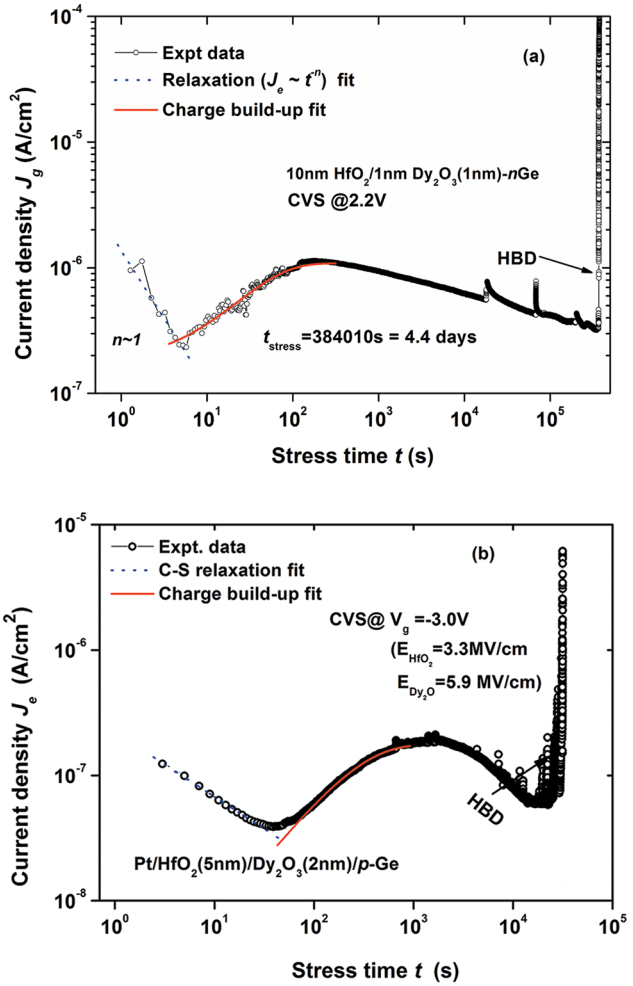

FIG. 7. Current density J_g as a function of stress time t for samples of HO_2/Dy_2O_3 gate stacks grown on n- and p- type Ge substrates at moderate CVS conditions applied for very long times. The device shows initially relaxation behavior, then (from $t > 12$ s for n-type, $t > 90$ s for p-type) charge trapping to the preexisting traps in the oxide takes place which eventually leads to breakdown.

(HfO_2) increases abruptly leading to a second relaxation effect. Hence, soft breakdown (SBD) effects appear, which eventually lead to a HBD of the second layer and the device itself. On the contrary, the single Dy_2O_3 layer (not shown here) needed a considerably longer time in order to collapse, probably due to the different breakdown mechanisms of the two oxides.

On the other hand, the application of very long CVS pulses on similar gate stacks (10 nm HfO_2/1 nm Dy_2O_3) but grown on n-type Ge substrates [see Fig. 7(b)] showed improved reliability characteristics. In particular, at moderate stress fields, (e.g., CVS at $V_g = 2.2$ V where $E_{HfO2} = 1.9$ MV/cm and $E_{Dy2O3} = 3.3$ MV/cm at $t_{stress} = 0$ s) it takes a very long time ($t = 38\,4000$ s i.e., 4.4 days) in order to observe breakdown characteristics. However, these gate stacks show similar behavior to their p-type substrates counterparts in the case of the J_g-t analysis. In that case, initially the current density decreases due to relaxation effects (C-S relaxation) for 6 s, followed by a negative charge trapping in the oxides.[17] In particular, the n value of the initial power law decay was calculated to be equal to unity, indicating the unimportance of M-W instabilities here. Furthermore, when the increasing part of the J_g-t transient was analyzed, the time constant τ for charge trapping was found to be 47 s signifying the presence of neutral traps[17,33] in the high-κ materials.

Therefore, a comparison of the results for the same gate stack configuration on both types of Ge-substrates illustrates the better quality of the n-type substrates in terms of electrical reliability. The superior quality of the devices grown on n-Ge substrates is in agreement with the well known problem of the p-Germanium surface properties as reported by many groups recently.[28] The latter, combined with the results presented in the previous sections (Sec. III D), conclude that the use of n-Ge substrates is suggested for better quality electrical characteristics for gate stack devices.

IV. CONCLUSIONS

The dielectric degradations and the electrical reliability characteristics of rare-earth oxides gate stacks grown on high mobility Ge substrates are studied by means of electrical measurements under CVS. Varying the applying voltage value (i.e., low to higher fields) while keeping the same polarity, trapping effects is observed at accumulation condition of the devices which is different from other SiO_2/Si systems. From border traps analysis we observe the "double peak" structure at the ΔN_{BT} curves which corresponds to both interface and border traps, which is also verified by complementary electrical measurements (C-$G_{p/\omega}$-V_g). The contribution of the interface traps at low bias is dominant to the other traps and influences the device degradation. We successfully propose a Maxwell-Wagner (M-W) mechanism in order to explain the decay current (J_g-t transient) at low to higher biases and it satisfies the experimental results. The mechanism for the breakdown of the gate REOs based stacks is also proposed using the assumption of M-W instabilities and progressive breakdown while finally the REOs degrade by a HBD. The different time constants of the charge trapping in the degradation of the gate stack based on n- and p-type Ge substrates, respectively, indicate the different nature of the defects. Analysis of the results shows that the uses of n-Ge substrates are suggested over p-Ge.

Finally, previously used M-W models had various constrains and weaknesses making difficult to explain the experimental data of longer J_g-t transient curves, while the temperature, field dependent and the frequency domain behavior of the relaxation parameters were not included into it. We are currently, working on the further development of the modified M-W model which takes into account the creation of new defects during CVS in the gate stacks which seems to explain better the experimental data.

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