Investigation of voltage dependent relaxation, charge trapping, and stress induced leakage current effects in HfO_2/Dy_2O_3 gate stacks grown on Ge (100) substrates

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Germanium is a very promising material and has an extra advantage due to its higher mobility than silicon. At the same time, high-κ gate dielectrics such as HfO_2 are already used for the replacement of SiO_2 in advanced complementary metal-oxide-semiconductor (MOS) devices. A buffer interfacial layer is required to have better interfacial quality between HfO_2 and the semiconductor substrate. In the present work the authors investigate the voltage dependent relaxation effects and charge trapping characteristics of $Pt/HfO_2/Dy_2O_3/p$-Ge MOS devices. The devices have been subjected to constant voltage stress and show relaxation effects in the whole range of applied stress voltages (-1 to -5 V). Charge trapping is negligible at low stress field while at higher fields (>4 MV/cm) it is significant. Also interesting is the fact that the trapped charge is negative at low stress fields but changes to positive at higher fields. © *2009 American Vacuum Society.* [DOI: 10.1116/1.3025912]

I. INTRODUCTION

Although the initial transistors were germanium based, over the past four decades silicon is the most widely utilized semiconductor for electronics. Pure Ge offers 2χ higher mobility for electrons and 4χ higher mobility for holes compared to Si. In order to keep up with scaling requirements set by ITRS, gate dielectrics with higher ($\sim$25) permittivity, such as HfO_2, are used as a replacement of SiO_2.[1] Germanium is highly reactive with HfO_2, which may lead to Ge diffusion into the HfO_2 dielectric.[1] One possible solution is the use of rare earth oxide dielectrics as passivation layers, which are "friendly" with Ge and can be directly deposited on it,[2] capped with a higher-κ dielectric to improve scalability. It has been shown that Dy_2O_3 can efficiently eliminate Ge diffusion originating either from the substrate or interfacial layer. It also reduces the charge trapping effects while improving the equivalent oxide thickness (EOT).[3]

Another serious problem that arises when gate stacks of high-κ dielectrics are used in metal-oxide-semiconductor (MOS) devices is that they all produce electrical instabilities in MOS devices.[4] This is a major device reliability issue since it causes threshold voltage (V_{th}) shifts and drive current degradation over device operation time. Many of these instabilities could be interpreted as arising from the trapping of charge somewhere within the gate stack. In particular, the high-speed experiments of Kerber *et al.*[5,6] seem to paint a vivid picture of electrons filling up a gate stack when a gate bias is applied, then rushing out after the bias is removed, producing dramatic instabilities in the drain current of transistors at short time scales. By cycling the gate voltage on and off,[4–6] one also observes gradual shifts in the properties of devices, implying that the electrons that flow into the gate stack while the bias is on do not have time to flow out completely when the bias is off. For high-κ gate stacks to be suitable for commercial devices, these electrical instabilities must be eliminated, so it is imperative to understand why charge trapping takes place.

Two effects are known to produce such instabilities in MOS devices, namely, the Maxwell–Wagner instability and the relaxation effects of the various gate dielectrics. They both give a $J \sim t^{-n}$ behavior, which is strongly voltage dependent.[4–7] Moreover, they are usually both present at the same time, making the corresponding analysis a very complex task. This is also the main subject of the present work. The studied $Pt/HfO_2/Dy_2O_3/p$-Ge MOS devices have been subjected to constant voltage stress (CVS) conditions at accumulation and they show Maxwell–Wagner instabilities and relaxation effects as well as charge trapping at pre-existing bulk oxide defects.

II. EXPERIMENT

Dy_2O_3/HfO_2 oxide stacks were prepared by atomic oxygen beam deposition on p-type Ge (100) substrates. Native oxide was desorbed *in situ* under UHV conditions by heating the substrate to 360 °C for 15 min until a (2×1) reconstruction appeared in the (reflection high-energy electron diffraction) pattern, indicating a clean (100) surface. Subsequently, the substrate was cooled down to 225 °C where the oxide stacks were deposited. The surface was exposed to atomic O beams generated by a rf plasma source with the simultaneous e-beam evaporation of Dy/Hf at a rate of about $\sim$0.15 Å/s. Two different samples were prepared for the present study. Sample A had a single ($\sim$10 nm thick) Dy_2O_3 layer while

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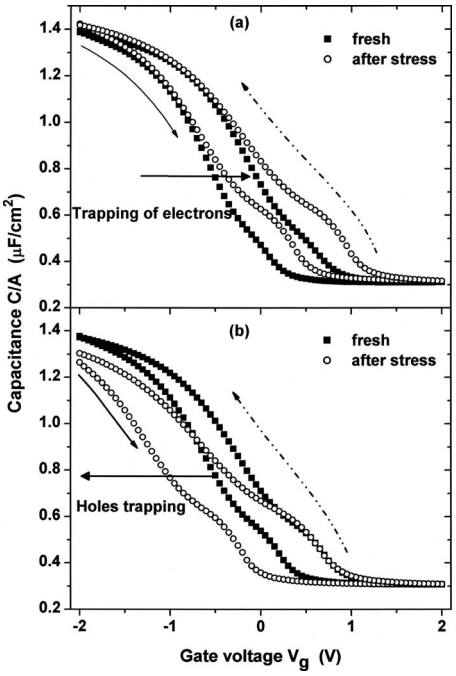

FIG. 1. High frequency *C-V* ($f=100$ kHz) before and after the application of ten consecutive CVS cycles of 500 s each on sample B (Pt–5 nm HfO_2/2 nm Dy_2O_3/*p*-Ge). Stress voltage is low in (a) and moderate in (b). Positive V_{FB} shifts in (a) indicate trapping of electrons in the bulk of the oxides while negative shifts in (b) indicate the opposite.

the total thickness of the dielectrics of sample B was approximately 7 nm (5 nm HfO_2/2 nm Dy_2O_3). MOS capacitors were prepared by shadow mask and e-beam evaporation of 30-nm-thick Pt electrodes to define circular dots, 200 μm in diameter. The back Ohmic contact was made using a eutectic InGa alloy.

The devices have been subjected to electrical stress under CVS conditions at accumulation. Successive stress cycles of 500 s at different gate voltages were applied with the Keithley 617 meter that was also measuring the corresponding current with time. After each stress cycle the gate bias was stopped in order to measure either the current-voltage (I_g-V_g) curves or the high frequency ($f=100$ kHz) capacitance-voltage (*C-V*) curve for the determination of the flatband voltage shift (ΔV_{FB}). The latter measurement was obtained with the Agilent 4284A *LCR* meter.

III. RESULTS AND DISCUSSION

Typical *C-V* curves of the MOS capacitor with the gate stack dielectric are illustrated in Figs. 1(a) and 1(b). In order to measure the trapped oxide charges immediately after stopping the stress pulse, the curves were obtained from accumulation to inversion and backward. Nevertheless, the important electrical properties of the capacitors do not show substantial differences from the *C-V*'s acquired in the opposite way (i.e., from inversion to accumulation and backward). Taking into account quantum mechanical corrections, the calculated EOT values were 2.68 and 1.93 nm for samples A and B, respectively. The hysteresis of *C-V* curve was rather large (around 400 mV at midgap) and a large density of slow interface traps is evident even at ac signal frequencies as high as 100 kHz. The corresponding current-voltage (*I-V*) curves show very small leakage currents (around 10 nA/cm^2 at $V_{FB}-1$ V). Important information comes from the structural analysis of the films, which evidences the presence of a thin amorphous interfacial layer consisting mainly of Ge–O–Dy phases. Hence both samples must be considered as gate stacks.

The interesting result from the analysis of the high frequency *C-V* curves [Figs. 1(a) and 1(b)] is that when the applied stress voltage is rather low, the trapped charge in the oxide is negative (i.e., ΔV_{FB} shift is positive), while at moderate stress voltages the relevant negative shift of the *C-V* curves indicates positive charge trapping. The same results have also been obtained for the single Dy_2O_3 layer. There are two possible explanations of the observed phenomenon:

(1) As the gate voltage during the stress pulse is always negative, electrons are injected into the dielectrics from the metal. At low voltages these electrons are trapped in preexisting defects and the fields across each dielectric are not high enough for these electrons to escape toward the *p*-Ge substrate (assuming the usual Poole–Frenkel or trap assisted tunneling transport). At higher stress voltages the situation is different in the sense that even the electrons already trapped in the oxides are able to escape toward the substrate, thus leaving a net positively charged dielectric.

(2) The fact that the two layers of a high-κ gate stack are different materials means that they also have different conductivities. Then, the application of a gate bias will immediately produce a discontinuity in current density at the interface between the two layers, causing charge to accumulate there until, in steady state, the same current density (J_e) flows through both layers. If the gate bias is removed, a discontinuity in current density will again be produced, this time causing the charge to rush out of the gate stack.[4] Another aspect worth noting is that because the conductivities of HfO_2 and Dy_2O_3 thin films depend differently on field, either layer can have the higher conductivity, depending on the choice of gate voltage. Frohman-Bentchkowsky and Lenzlinger[8] caused the sign of the trapped charge to switch by varying the gate voltage of similar (gate stack) structures. This effect was predicted from the independent measurements of the conductivities of the two layers.[4,8] Similar changes of sign might have already been observed in HfO_2/SiO_2 gate stacks.[8] Furthermore, in a previous work,[9] we observed the same effect on MOS devices with CeO_2 as the gate dielectric.

In order to understand better which mechanism is responsible for the voltage dependence of ΔV_{FB}, the transient response of the current during the application of the stress pulse was measured. Figures 2(a) and 2(b) illustrate the current density J_e versus stress time t curves after the application of low gate voltage pulses on both samples. It is evident that in all cases, the decay of current follows a t^{-n} law with n values ranging from 0.5 to 1. Additionally, the n values increase after each new stress cycle, reaching a value of 0.9

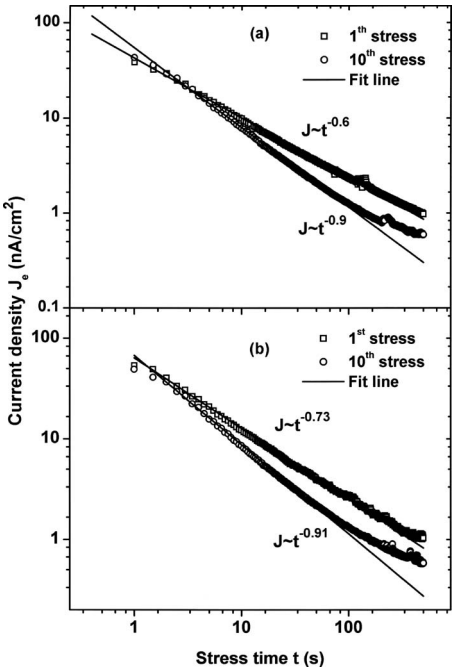

FIG. 2. The figures illustrate absolute current density J_e as a function of stress time t. Comparison of transient current behavior during the application of the first and the tenth stress pulses. The applied gate voltage bias and the corresponding fields are low for both samples (A and B). The solid lines show the corresponding t^{-n} behavior.

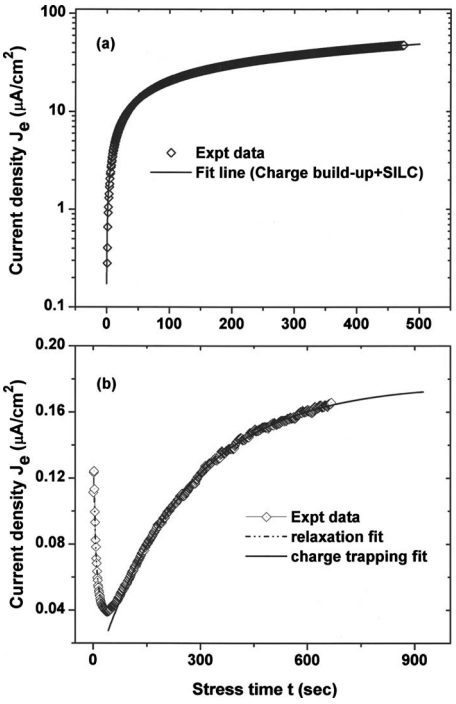

FIG. 3. Figures show the absolute J_e vs t, the comparison of the transient current behavior during the application of a stress pulse at a higher gate voltage bias so that the corresponding fields are moderate for both samples A and B [(a) and (b), respectively]. The solid lines are best fit to the experimental data according to a model described in the text.

after ten cycles. The fact that the initial value is far from unity indicates that a Maxwell–Wagner instability (following the terminology used in Ref. 4) is present along with the usual dielectric relaxation of the high-κ dielectrics. In the latter case the relaxation current decays with time following the Curie–von Schweidler law:[10] $J_e/P=\alpha t^{-n}$, where J_e is the relaxation current density $(\mathrm{A/cm^2})$, P is the total polarization or surface charge density $(\mathrm{V\,nF/cm^2})$, α is a constant in seconds, and n is a real number close to 1. The gradual increase of n could be attributed to the fact that the Maxwell–Wagner instability becomes less important after each stress cycle and the relevant J_e values decrease so that, after ten consecutive cycles, it is the dielectric relaxation current that dominates. One reason for that is the gradual change of the conductivities of the various dielectric layers due to charge trapping in pre-existing bulk oxide defects. Another observation supporting the above analysis is the fact that the initial n value of sample B is considerably higher than that of sample A. The former structure contains a HfO_2 layer with a higher dielectric constant ($\kappa\sim 25$) than that of Dy_2O_3. Therefore the dielectric relaxation effects are expected to be stronger in the case of sample B.

The situation is different at higher applied voltages. As illustrated in Fig. 3, the application of moderate to high stress voltages does not result in relaxation effects for the MOS device with the single Dy_2O_3 film (sample A). The transient current behavior is now governed by charge trapping at pre-existing bulk oxide defects. On the contrary, application of similar stress voltages on the capacitor with the HfO_2/Dy_2O_3 stack shows the coexistence of all different mechanisms separated only by the different time scales of each one. Therefore, during the first 32 s after the application of the pulse, the current density J_e decreases with time due to the relaxation mechanisms, following a t^{-n} law with n values as low as 0.5. At the same time the magnitude of the leakage current that flows through the dielectrics is two to three orders of magnitude higher than that in the case of low stress voltages. Therefore the charge trapping effects become more significant and the J_e values start to increase, following a model originally proposed by Nigam *et al.*[11] to explain charge trapping in MOS devices with thin gate stack dielectrics. According to this model, the transient behavior of J_e with time of sample A [Fig. 3(a)] can be explained by taking into consideration both trapping on pre-existing bulk oxide defects (with a characteristic time constant τ) as well as creation of new defects due to electrical stressing (which follow a power law $J_e\sim t^{\delta}$). However, for sample B, only charge trapping must be considered for best fitting of the experimental data [Fig. 3(b)]. In addition, the time constant τ is one order of magnitude greater ($\tau\sim 260$ s) for sample B than for the structure containing only Dy_2O_3. This is an interesting result as it shows that there are different types of defects in the two oxides. Furthermore, the overall better insulating properties of HfO_2 are confirmed as sample B, although stressed at slightly higher electric fields, shows negligible rate of creation of new defects.

Finally both devices have been subjected to very long CVS conditions at moderate gate voltages. Figure 4 shows that sample B reaches hard breakdown after a number of soft

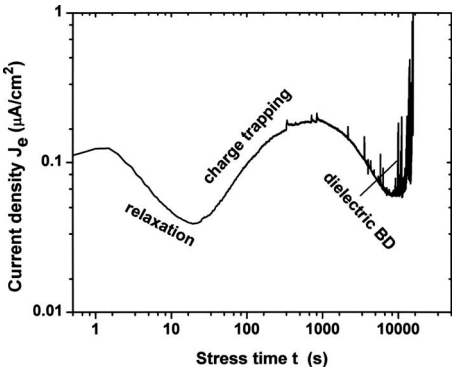

FIG. 4. Current density J_e as a function of stress time t for sample B at moderate/high CVS conditions applied for very long times. The device initially shows relaxation behavior, then (for $t>90$ s) charge trapping to the pre-existing traps in the oxide takes place, which eventually leads to breakdown.

breakdown events and a total stress time of 18 000 s. On the contrary the single Dy_2O_3 layer (not shown here) required substantially longer periods of time in order to collapse, which is probably attributed to the different breakdown mechanisms occurring in the two oxides. One possible explanation is that in the case of the gate stack dielectric, one of the oxides (most probably the thinner Dy_2O_3) goes to breakdown first, leading to a major redistribution of the corresponding fields. Thus the field across the other dielectric (HfO_2) increases abruptly, leading to a second relaxation effect. This time soft breakdown effects appear, which eventually lead to a hard breakdown of the second layer and the MOS capacitor itself. Nevertheless this effect needs to be studied in more detail.

IV. CONCLUSION

Charge trapping and relaxation characteristics of $Pt/HfO_2/Dy_2O_3/p$-Ge gate stacks were studied by means of CVS measurements. At low applied stress voltages two independent electrical instabilities were observed, namely, the Maxwell–Wagner instability and dielectric relaxation. While both effects were present simultaneously, the increase of the applied voltage and/or the repetition of the stress cycles lead to a change of the relative magnitude of each one separately.

Another aspect of the studied structures worth noting is that because the conductivities of HfO_2 and Dy_2O_3 thin films depend differently on field, either layer can have the higher conductivity, depending on the choice of gate voltage. Then, by varying the gate voltage, the sign of the trapped charge switched from positive to negative, an effect that was predicted but rarely reported for high-κ gate stacks. Finally, at moderate to high stress fields the dominant process is charge trapping and creation of new defects (SILC). The analysis of the transient behavior of the current density in this case revealed the existence of two different trapping centers in the two dielectrics at least in terms of the relevant capture cross sections.

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